

EE 330

Lecture 44

Digital Circuits

- Dynamic Logic Circuits
- Higher-level digital blocks

Fall 2024 Exam Schedule

Exam 1	Friday	Sept 27
Exam 2	Friday	October 25
Exam 3	Friday	Nov 22
Final Exam	Monday	Dec 16 12:00 - 2:00 PM

Final Exam Attachments

MOSIS WAFER ACCEPTANCE TESTS

RUN: T68B (MM_NON-EPI) VENDOR:
TSMC TECHNOLOGY: SCN018 FEATURE SIZE: 0.18 microns

COMMENTS: DSCN6M018_TSMC

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM Vth	0.27/0.18	0.50	-0.51	volts
SHORT Idss	20.0/0.18	547	-250	uA/um
Vth		0.51	-0.51	volts
Vpt		4.8	-5.6	volts
WIDE Ids0	20.0/0.18	14.4	-4.7	pA/um
LARGE Vth	50/50	0.43	-0.42	volts
Vjblk		3.1	-4.3	volts
Ijlk		<50.0	<50.0	pA
K' (Uo*Cox/2)		175.4	-35.6	uA/V^2
Low-field Mobility		416.52	84.54	cm^2/V*s

PROCESS PARAMETERS	N+	P+	POLY	N+BLK	PLY+BLK	M1	M2	UNITS
Sheet Resistance	6.7	7.8	8.0	59.7	313.6	0.08	0.08	ohms/sq
Contact Resistance	10.6	11.0	10.0					4.79 ohms
Gate Oxide Thickness	41							angstrom

PROCESS PARAMETERS	M3	POLY_HRI	M4	M5	M6	N W	UNITS
Sheet Resistance	0.08		0.08	0.08	0.03	930	ohms/sq
Contact Resistance	9.24		14.05	18.39	20.69		ohms

CAPACITANCE PARAMETERS	N+	P+	POLY	M1	M2	M3	M4	M5	M6	R_W	D_N W	MSP	N W	UNITS
Area (substrate)	942	1163	106	34	14	9	6	5	3		123		125	aF/um^2
Area (N+active)			8484	55	20	13	11	9	8					aF/um^2
Area (P+active)			8232											aF/um^2
Area (poly)				66	17	10	7	5	4					aF/um^2
Area (metall1)				37	14	9	6	5						aF/um^2
Area (metall2)					35	14	9	6						aF/um^2
Area (metall3)						37	14	9						aF/um^2
Area (metall4)							36	14						aF/um^2
Area (metall5)								34					984	aF/um^2
Area (r well)	920													aF/um^2
Area (d well)									582					aF/um^2
Area (no well)	137													aF/um^2
Fringe (substrate)	212	235		41	35	29	21	14						aF/um
Fringe (poly)				70	39	29	23	20	17					aF/um
Fringe (metall1)					52	34		22	19					aF/um
Fringe (metall2)						48	35	27	22					aF/um
Fringe (metall3)							53	34	27					aF/um
Fringe (metall4)								58	35					aF/um
Fringe (metall5)									55					aF/um
Overlap (N+active)			895											aF/um
Overlap (P+active)			737											aF/um



Basic Amplifier Gain Table

Configuration	BJT	MOS	BJT	MOS	BJT	MOS	BJT	MOS	BJT	MOS
A_V	$-\frac{I_{CQ}R_C}{V_i}$	$-\frac{g_m R_D}{V_i}$	$\frac{I_{CQ}R_C}{V_i}$	$\frac{g_m R_C}{V_i}$	$-\frac{g_m R_C}{g_m + g_e}$	$\frac{2I_{DQ}R_C}{2I_{DQ}R_E + V_{EB}}$	$9mR_C$	$9mR_C$	$-\frac{RC}{RE}$	$\frac{2I_{DQ}R_C}{V_{EB}}$
R_{in}	$\beta \frac{V_i}{I_{CQ}}$	r_{π}	$\beta \left(\frac{V_i}{I_{CQ}} + R_E \right)$	$\beta \left(\frac{V_i}{I_{CQ}} + R_E \right)$	$r_{\pi} + \beta R_E$	∞	$\frac{V_i}{I_{CQ}}$	$\frac{V_i}{I_{CQ}}$	∞	$\frac{V_{EB}}{2I_{DQ}}$
R_{out}	R_C	R_C	R_C	R_C	R_C	R_C	R_C	R_C	R_C	R_C

Final Exam Attachments

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Propagation Delay in Logic Circuits with OD and Asymetry



	Equal Rise/Fall	Equal Rise/Fall (with OD)	Minimum Sized	Asymmetric OD (OD _{HL} , OD _{LH})
C_{IN}/C_{REF}				
Inverter	1	OD	1/2	$\frac{OD_{HL} + 3 \cdot OD_{LH}}{4}$
NOR	$\frac{3k+1}{4}$	$\frac{3k+1}{4} \cdot OD$	1/2	$\frac{OD_{HL} + 3k \cdot OD_{LH}}{4}$
NAND	$\frac{3+k}{4}$	$\frac{3+k}{4} \cdot OD$	1/2	$\frac{k \cdot OD_{HL} + 3 \cdot OD_{LH}}{4}$
Overdrive				
Inverter HL	1	OD	1	OD _{HL}
LH	1	OD	1/3	OD _{LH}
NOR HL	1	OD	1	OD _{HL}
LH	1	OD	1/(3k)	OD _{LH}
NAND HL	1	OD	1/k	OD _{HL}
LH	1	OD	1/3	OD _{LH}
t_{PROP}/t_{REF}	$\sum_{k=1}^n F_{1(k+1)}$	$\sum_{k=1}^n \frac{F_{1(k+1)}}{OD_k}$	$\frac{1}{2} \sum_{k=1}^n F_{1(k+1)} \left(\frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right)$	$\frac{1}{2} \sum_{k=1}^n F_{1(k+1)} \left(\frac{1}{OD_{HLk}} + \frac{1}{OD_{LHk}} \right)$

Dc and small-signal equivalent elements

	Element	ss equivalent	dc equivalent
dc Voltage Source	V_{DC} [Symbol]	[Symbol]	V_{DC} [Symbol]
ac Voltage Source	V_{AC} [Symbol]	V_{AC} [Symbol]	[Symbol]
dc Current Source	I_{DC} [Symbol]	[Symbol]	I_{DC} [Symbol]
ac Current Source	I_{AC} [Symbol]	I_{AC} [Symbol]	[Symbol]
Resistor	R [Symbol]	R [Symbol]	R [Symbol]

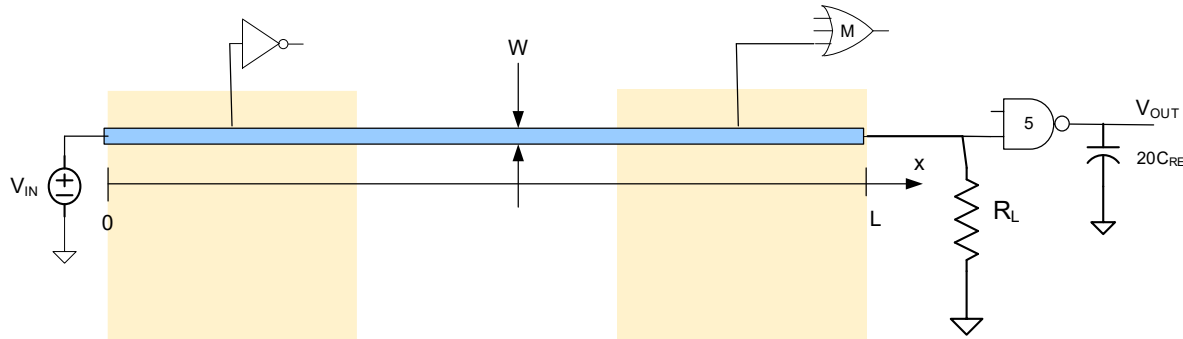
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	Element	ss equivalent	dc equivalent
Capacitors	Large C [Symbol]	[Symbol]	[Symbol]
	Small C [Symbol]	C [Symbol]	[Symbol]
Inductors	Large L [Symbol]	[Symbol]	[Symbol]
	Small L [Symbol]	L [Symbol]	[Symbol]
Diodes	[Symbol]	[Symbol]	[Symbol] Simplified
	[Symbol]	[Symbol]	[Symbol] Simplified
MOS transistors	[Symbol]	[Symbol]	[Symbol] Simplified
	[Symbol]	[Symbol]	[Symbol] Simplified

	Element	ss equivalent	dc equivalent
Bipolar Transistors	[Symbol]	[Symbol]	[Symbol] Simplified
	[Symbol]	[Symbol]	[Symbol] Simplified
Dependent Sources	[Symbol]	[Symbol]	[Symbol]
	[Symbol]	[Symbol]	[Symbol]

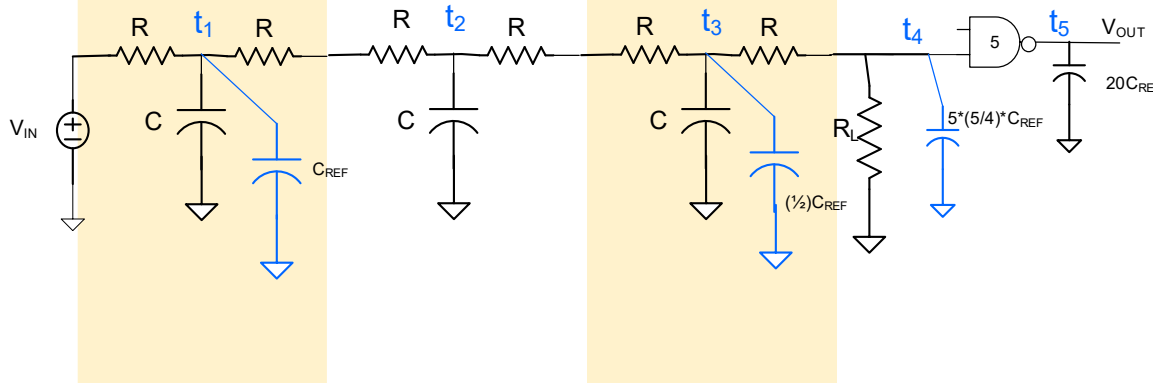
Elmore Delay Calculations

Determine propagation delay



$$R = \frac{1}{6} R_{\square} \frac{L}{W}$$

$$C = \frac{1}{3} C_D$$



$$t_1 = R(C + C_{REF}) \quad t_2 = 3RC \quad t_3 = 5R\left(C + \frac{1}{2}C_{REF}\right) \quad t_4 = [6R \parallel R_L] \frac{25}{4} C_{REF} \quad t_{PROP5} = t_{REF} \frac{20}{5}$$

$$t_{PROP} = 2 \sum_{i=1}^4 t_i + t_{PROP5}$$

Power Dissipation in Logic Circuits

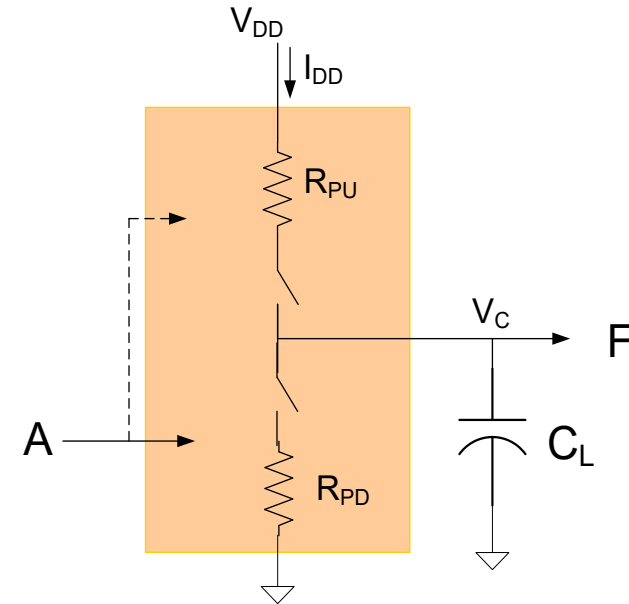
Types of Power Dissipation

- **Static**
- **Pipe**
- **Dynamic**
- **Leakage**
 - **Gate**
 - **Diffusion**
 - **Drain**

Dynamic Power Dissipation

Energy dissipated with clock signal itself

$$P_{DYN} = f_{CL} C_L V_{DD}^2$$

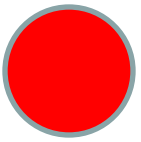


The clock transitions on every clock cycle (i.e. it has a transition duty cycle of 100%)

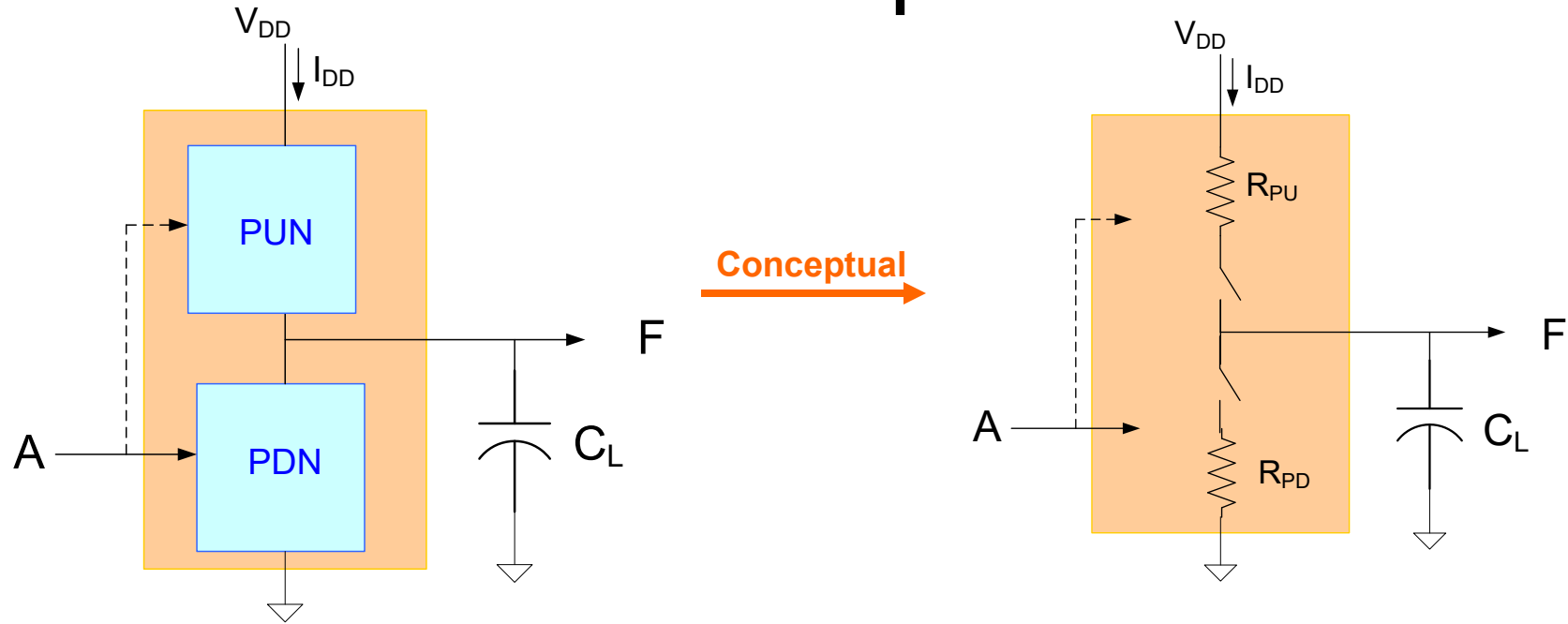
Clock distribution can cause significant power dissipation

But if a gate has a transition duty cycle of 50% with a clock frequency of f_{CL}

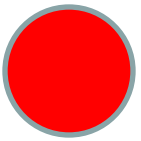
$$P_{DYN} = \frac{f_{CL}}{2} C_L V_{DD}^2$$



Power Dissipation



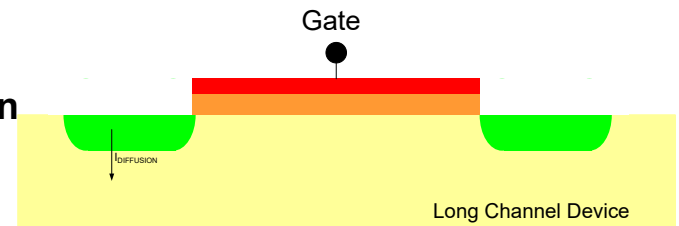
- All power is dissipated in pull-up and pull-down devices
- C_L dissipates no power but PUN and PDN dissipate power when charging and discharging C_L
- Dynamic power dissipation reduced by more (often much more) than a factor of 2 if minimum sizing strategy is used
- NAND logic more attractive than NOR logic when multiple inputs required



Leakage Power Dissipation

- Gate

- with very thin gate oxides, some gate leakage current flows
- major concern in 60nm and smaller processes
- actually a type of static power dissipation

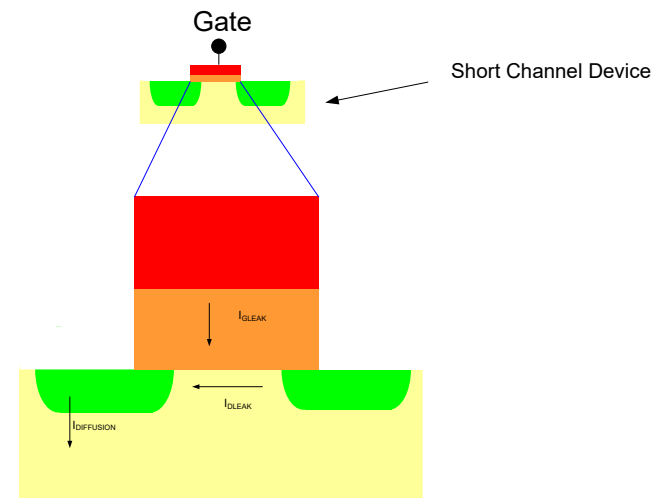


-Diffusion

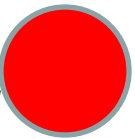
- Leakage across a reverse-biased pn junction
- Dependent upon total diffusion area
- May actually be dominant power loss on longer-channel devices
- Actually a type of static power dissipation

-Drain

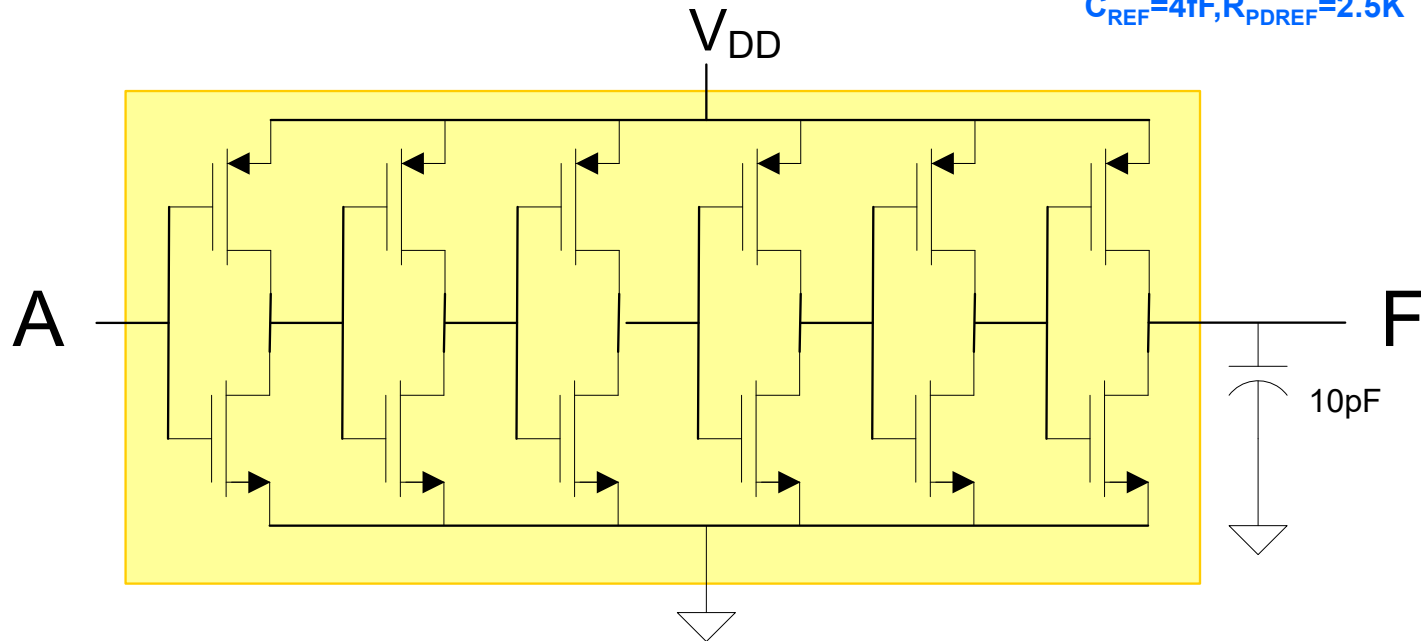
- channel current due to small $V_{\text{GS}} - V_{\text{T}}$
- of significant concern only with low V_{DD} processes
- actually a type of static power dissipation



Example: Determine the dynamic power dissipation in the last stage of a 6-stage CMOS pad driver if used to drive a 10pF capacitive load if the system clock is 500MHz and the output changes with 50% of the clock transitions. Assume pad driver with OD of $\theta=2.5$ and $V_{DD}=3.5V$



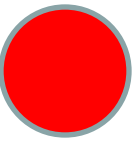
In 0.5u proc $t_{REF}=20ps$,
 $C_{REF}=4fF, R_{PDREF}=2.5K$



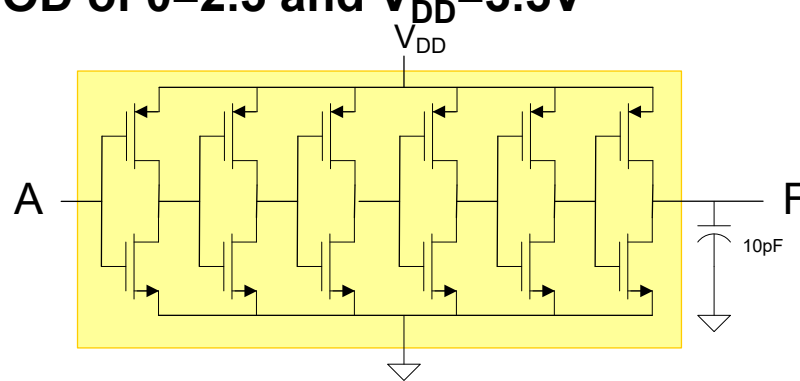
Solution: (assume output changes with 50% of clock transitions)

$$P_{DYN} = \frac{f_{CL}}{2} C_L V_{DD}^2 = \frac{5E8}{2} \cdot 10pF \cdot 3.5^2 = 30.5 \text{ mW}$$

Note this solution is independent of the OD and the process parameters
 (but decreases with advanced nodes because VDD goes down)



Example: Determine the power that would be required in the last stage of a CMOS pad driver to drive a 32-bit data bus off-chip if the capacitive load on each line is 10pF. Assume the clock speed is 500MHz and that each bit has an average 50% toggle rate. Assume a pad driver with OD of $\theta=2.5$ and $V_{DD}=3.5V$



In 0.5u proc $t_{REF}=20ps$,
 $C_{REF}=4fF, R_{PDREF}=2.5K$

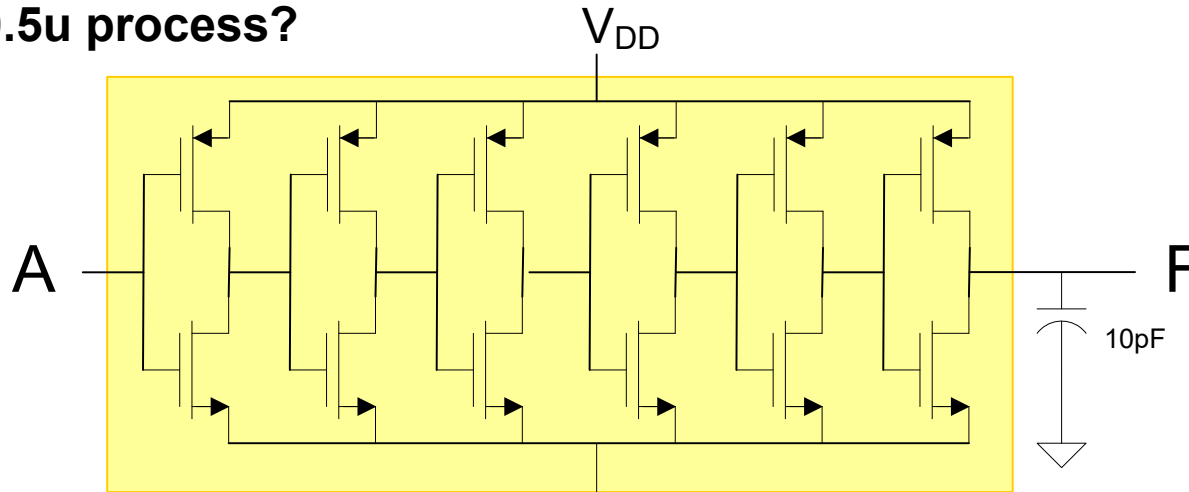
Solution:

$$P_{DYN} = 32 \cdot \frac{f_{CL}}{2} C_L V_{DD}^2 = 32 \cdot \frac{5E8}{2} \cdot 10pF \cdot 3.5^2 = 980mW$$

Note: A very large amount of power is required to take a large bus off-chip if bus has a high rate of activity.

Example: Will the CMOS pad driver actually be able to drive the 10pF load with a system clock of 500MHz as in the previous example in the 0.5u process?

In 0.5u proc $t_{REF}=20ps$,
 $C_{REF}=4fF, R_{PDREF}=2.5K$



Solution – since outputs are data dependent, output must be able to operate 500Mz:

$$t_{CLK} = \frac{1}{500MHz} = 2nsec$$

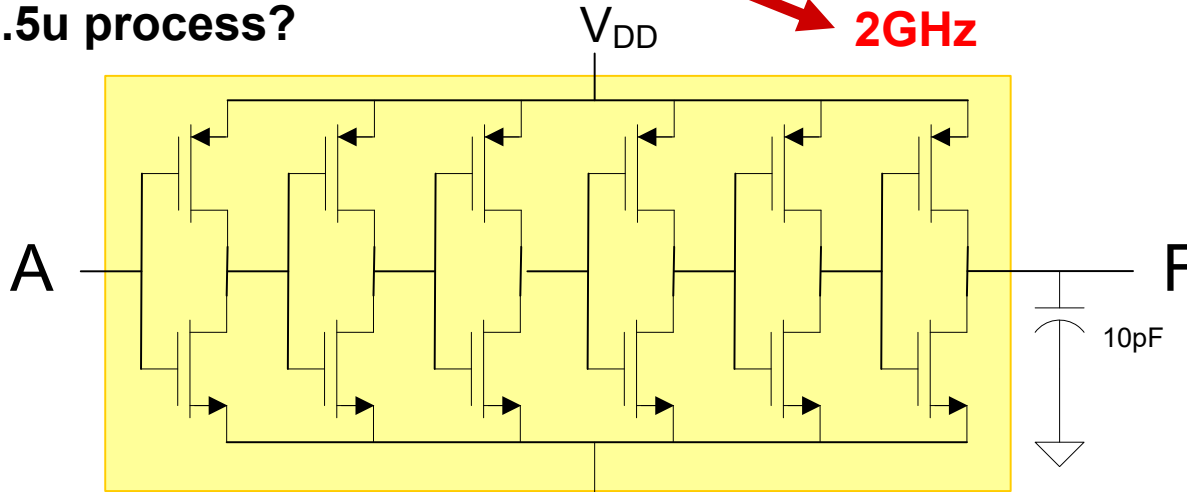
$$F_{load} = \frac{10pF}{4fF} = 2500 \quad OD_6 = \theta^5 = 98$$

$$t_{PROP} = 5\theta \cdot t_{REF} + \frac{F_{load}}{OD_6} t_{REF} \quad \frac{F_{load}}{OD_6} = \frac{2500}{98} \approx 25$$

$$t_{prop} = 5 \cdot 2.5 \cdot 20psec + 25 \cdot 20psec = (12.5 + 25) 20psec = 0.75nsec$$

since $t_{CLK} > t_{PROP}$, this pad driver can drive the 10pF load at 500MHz

Example: Will the CMOS pad driver actually be able to drive the 10pF load with a system clock of 500MHz as in the previous example in the 0.5u process?



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$$t_{CLK} = \frac{1}{500MHz} = 2nsec$$

~~500MHz~~ **2GHz** **0.5nsec**

$$F_{load} = \frac{10pF}{4fF} = 2500 \quad OD_6 = \theta^5 = 98$$

$$t_{PROP} = 5 \cdot \theta \cdot t_{REF} + \frac{F_{load}}{OD_6} t_{REF}$$

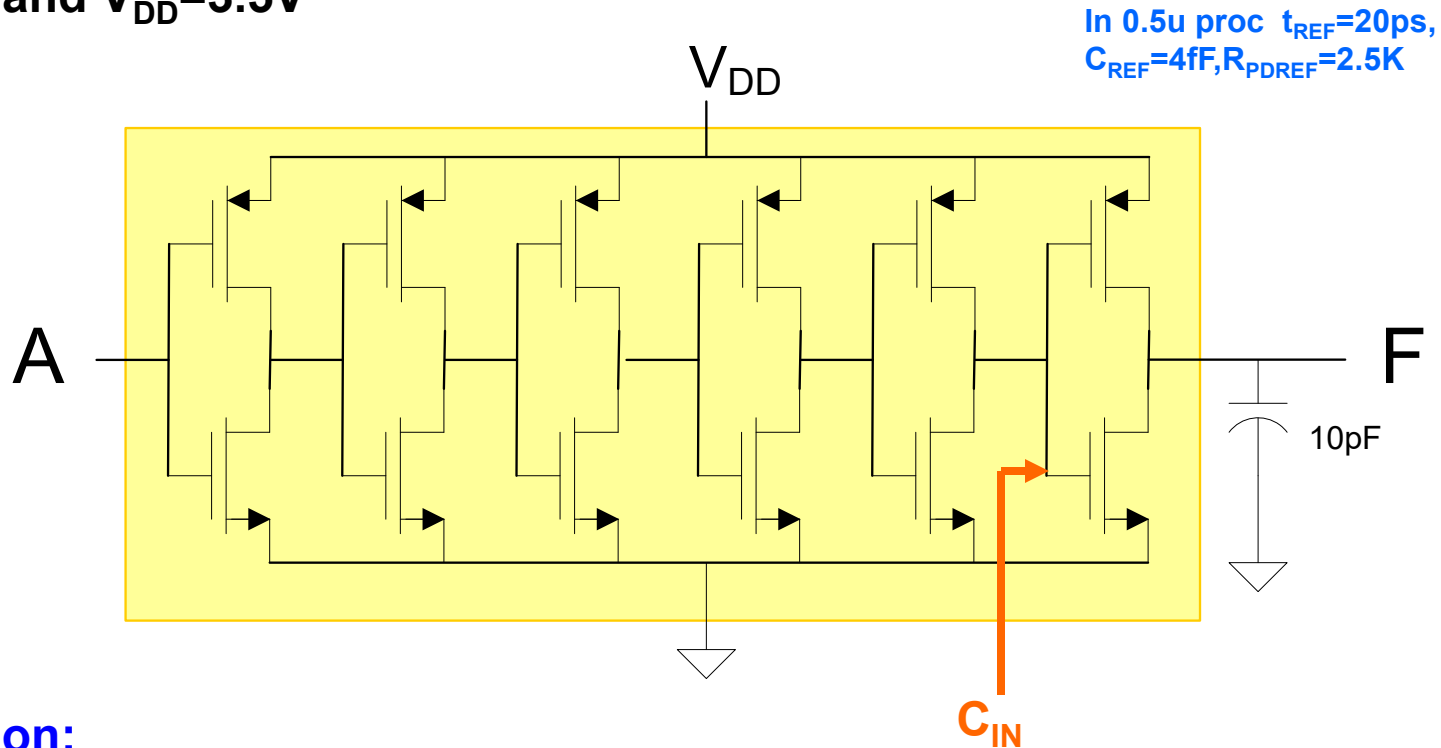
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since $t_{CLK} > t_{prop}$, this pad driver can drive the 10pF load at 500MHz

~~$t_{CLK} > t_{prop}$~~ **$t_{CLK} < t_{prop}$** **can not** **15 2GHz**

Example: Determine the dynamic power dissipation in the next to the last stage of a 6-stage CMOS pad driver if used to drive a 10pF capacitive load if clocked at 500MHz. Assume pad driver with OD of $\theta=2.5$ and $V_{DD}=3.5V$

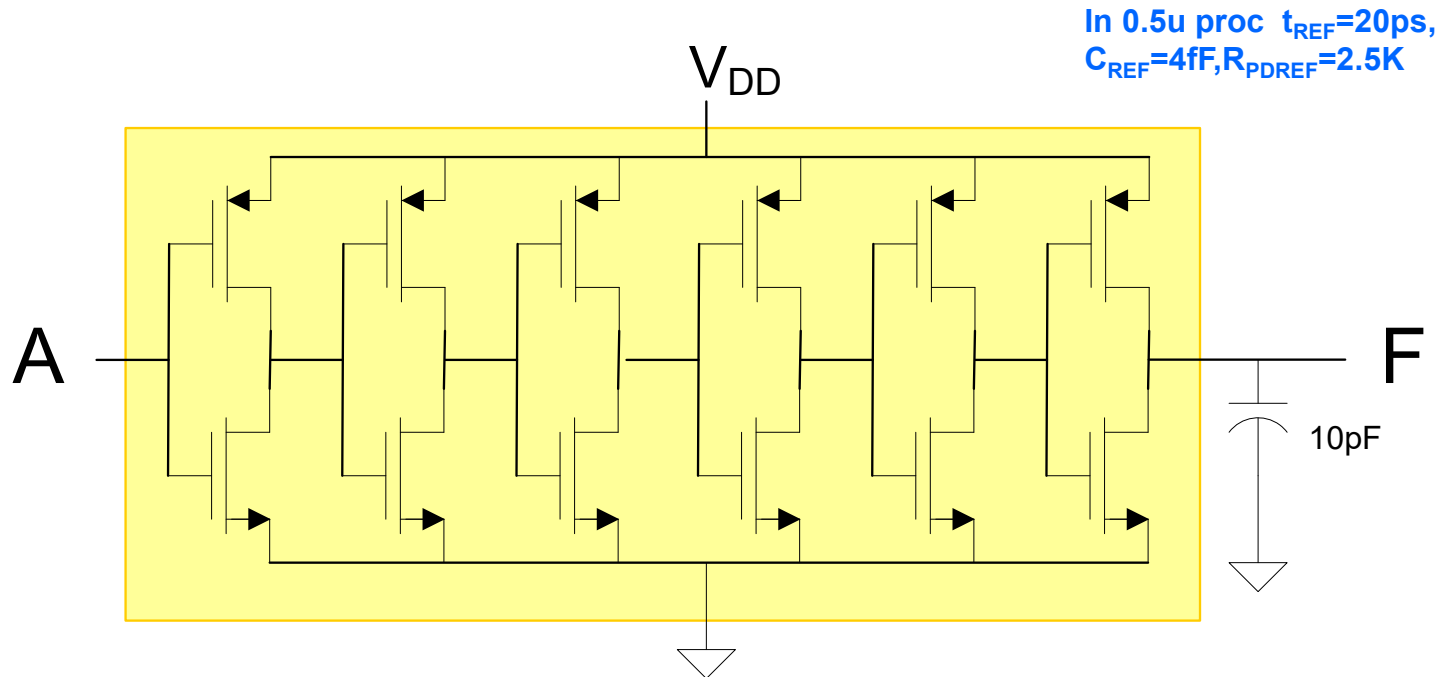


Solution:

$$C_{IN} = \theta^5 C_{REF} = 2.5^5 \cdot 4\text{fF} = 390\text{fF}$$

$$P_{DYN} = f_{CL} C_L V_{DD}^2 = 5\text{E}8 \cdot 390\text{fF} \cdot 3.5^2 = 2.4\text{mW}$$

Example: Is the 6-stage CMOS pad driver adequate to drive the 10pF capacitive load as fast as possible? Assume pad driver with OD of $\theta=2.5$ and $V_{DD}=3.5V$



Solution:

$$n_{OPT} = \ln\left(\frac{C_L}{C_{REF}}\right) = \ln\left(\frac{10pF}{4fF}\right) = 7.8$$

No – an 8-stage pad driver would drive the load much faster (but is not needed if clocked at only 500MHz)

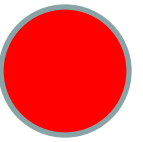
Digital Circuit Design

- Hierarchical Design
- Basic Logic Gates
- Properties of Logic Families
- Characterization of CMOS Inverter
- Static CMOS Logic Gates
 - Ratio Logic
- Propagation Delay
 - Simple analytical models
 - FI/OD
 - Logical Effort
 - Elmore Delay
- Sizing of Gates
 - The Reference Inverter

- Propagation Delay with Multiple Levels of Logic
- Optimal driving of Large Capacitive Loads
- Power Dissipation in Logic Circuits
- Other Logic Styles
 - Array Logic
 - Ring Oscillators

→ **done**

→ **partial**



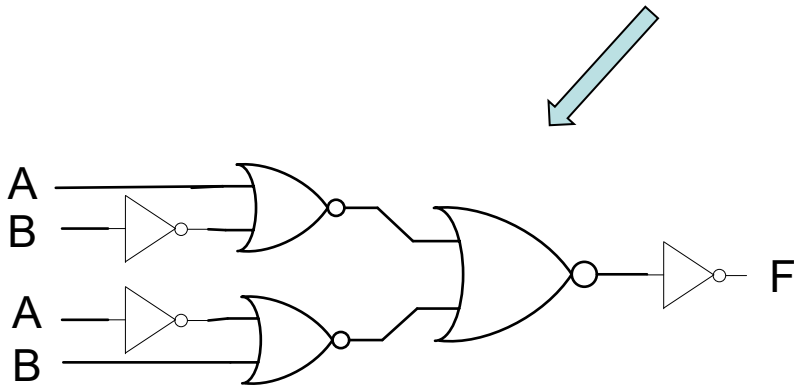
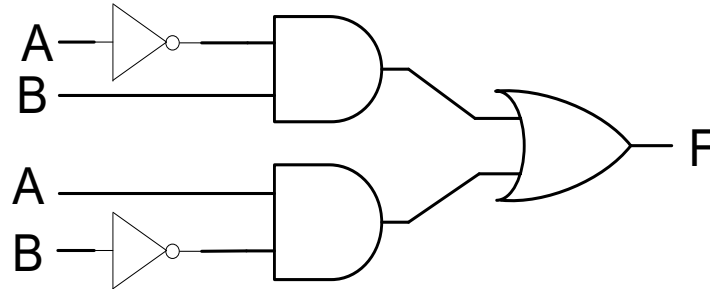
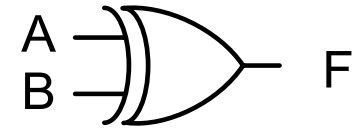
Logic Styles

- Static CMOS
- Complex Logic Gates
- Pass Transistor Logic (PTL)
- Pseudo NMOS
- Dynamic Logic
 - Domino
 - Zipper

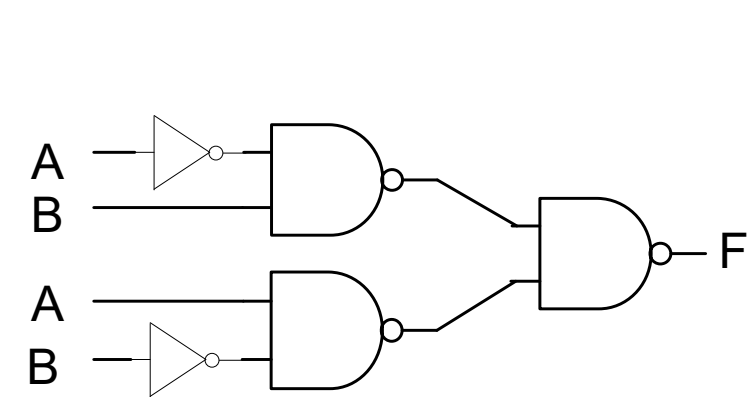
Static CMOS

Example: $F=A \oplus B$

$$F=A\bar{B}+\bar{A}B$$



18 transistors, 4 levels of logic



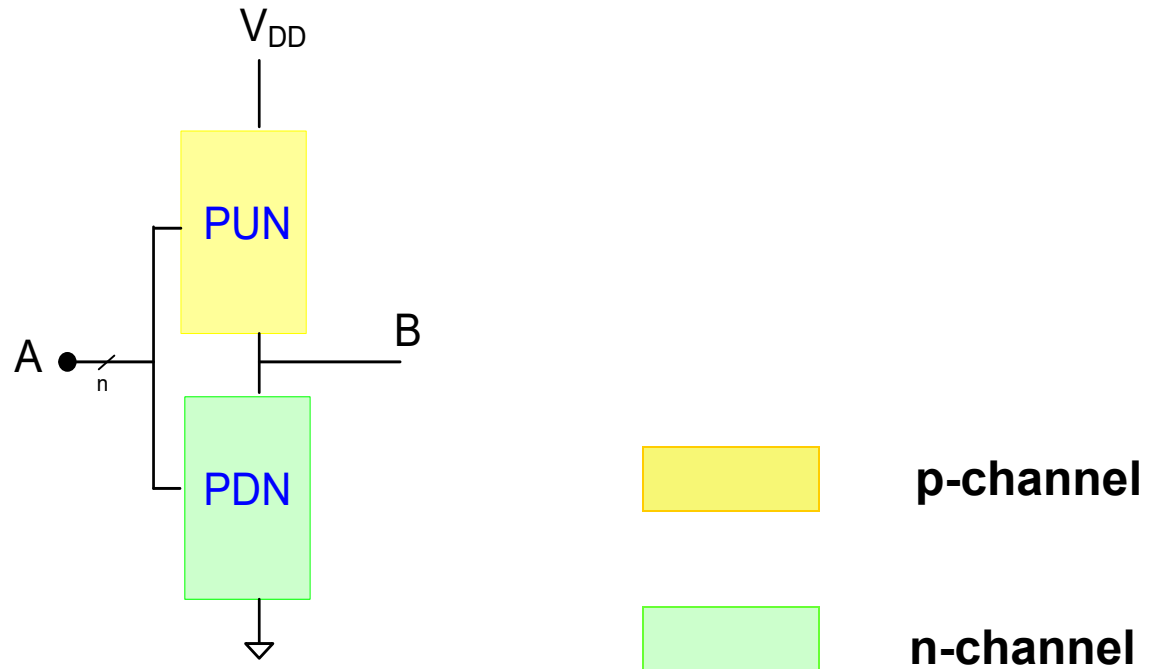
16 transistors, 3 levels of logic

Number of devices is unacceptably large in some applications

Dynamic Power Dissipation can be large, in particular for multiple-input NOR gates because of their large Fan In

Static CMOS Logic Gates

Any multiple-input NAND or NOR gate can be represented as:



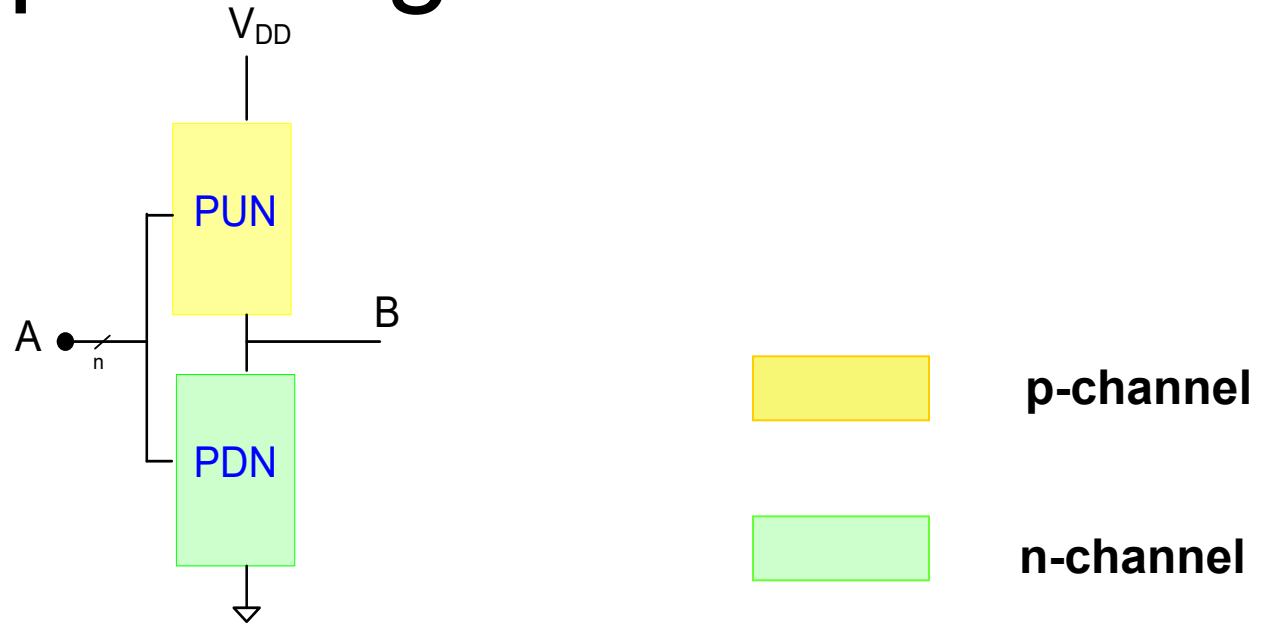
- Implement \overline{B} in PUN
- Implement B in PDN with complimented input variables
- Zero static power dissipation
- $V_H = V_{DD}$, $V_L = 0V$ (or V_{SS})
- Complimented input variables often required

Have implemented the logical function twice (once in PU, again in PD) and this is a major contributor to increased area and dynamic power dissipation

Logic Styles

- Static CMOS
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Complex Logic Gates



- Implement B in PDN
- Implement B in PUN with complemented input variables
- Zero static power dissipation
- $V_H = V_{DD}$, $V_L = 0V$ (or V_{SS})
- Complemented input variables often required

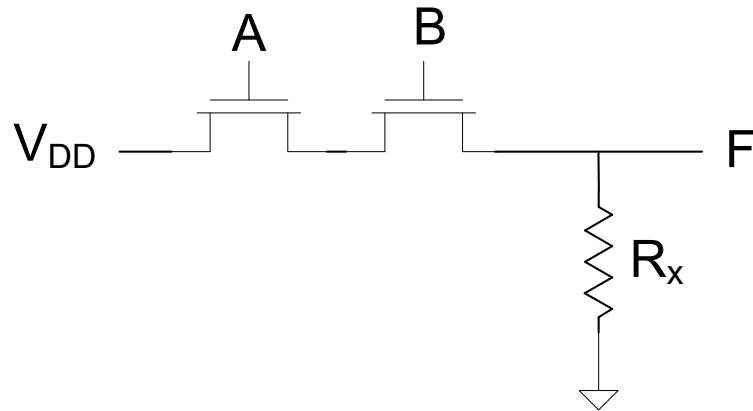
Can reduce the number of levels of logic and the total device count for some functions

Have implemented the logical function twice (once in PU, again in PD) and this is a major contributor to increased area and dynamic power dissipation

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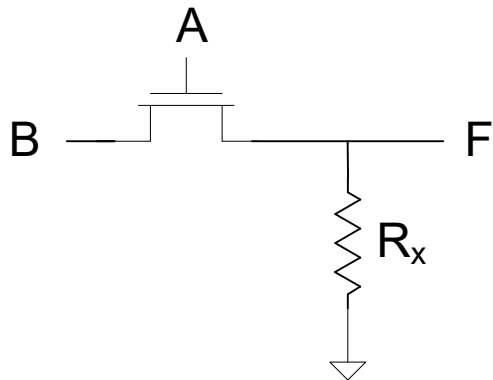
Pass Transistor Logic



$$F=AB$$

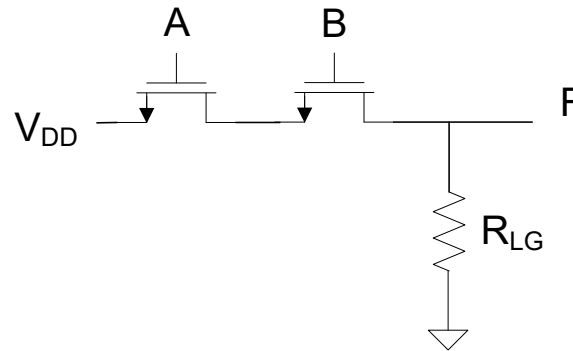
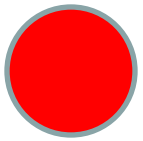
AND Gate

Requires only 3 components



Even simpler AND gate, requires only 2 components

Pass Transistor Logic



$$F=A \cdot B$$

Observations about PTL

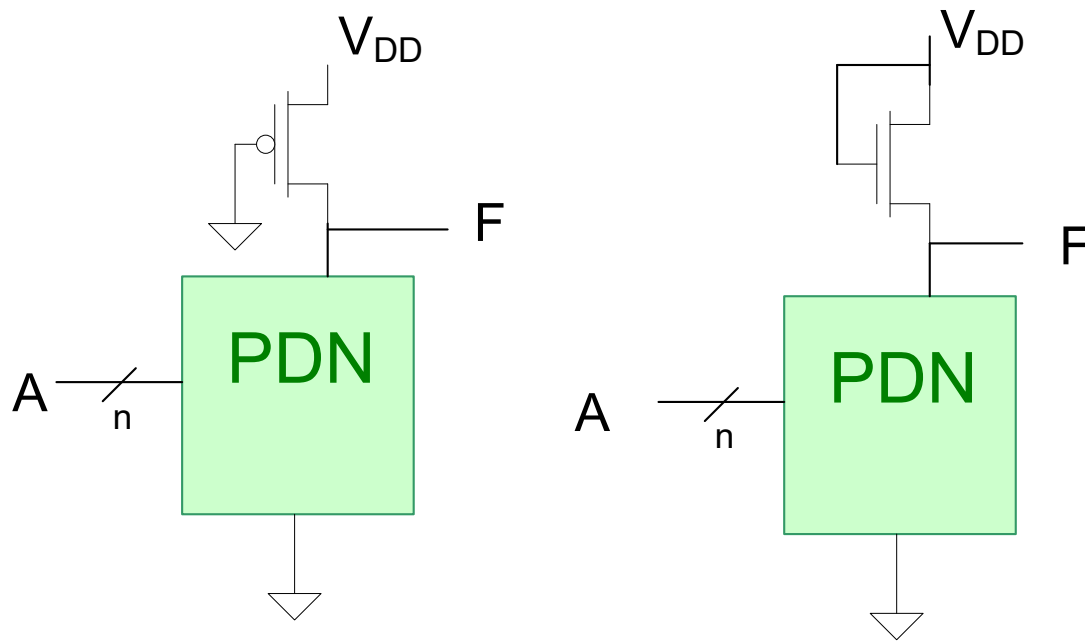
- Low device count implementation of non inverting function (can be dramatic) 😊
- Logic Swing not rail to rail 😞
- Static power dissipation not 0 when F high 😞
- R_{LG} may be unacceptably large 😞
- Slow t_{LH} 😞
- Signal degradation can occur when multiple levels of logic are used 😞
- Widely used in some applications 😊
- Implements basic logic function only once! 😊
- Fan In can be very small – so low dynamic power dissipation ! 😊

Is there a way to take advantage of the dynamic power dissipation advantages of a small fan-in without the dramatic energy penalty of a large static power dissipation?

Logic Styles

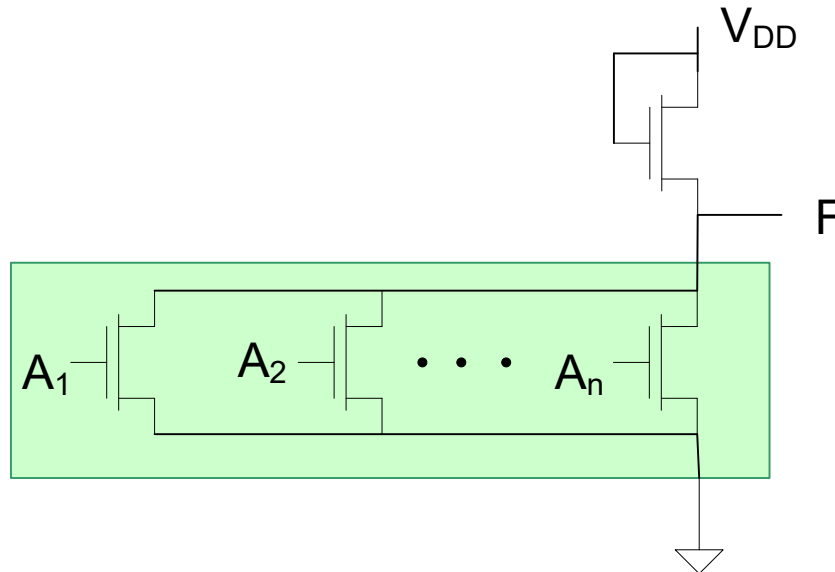
- Static CMOS
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Pseudo NMOS Logic



- May be viewed as a special case of PTL
- Ratioed Logic
- Static power dissipation not 0 (in PD state)
- Often used for really large number of inputs – e.g. NOR
- Only one additional transistor for each additional Boolean input
- Would be particularly useful for identifying one (or more) of many events that occur very infrequently

Pseudo NMOS Logic



n could be several hundred or even several thousand

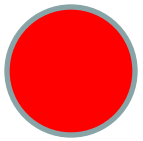
Static power dissipation independent of the number of inputs

May justify paying the static power dissipation penalty if a large number of inputs are needed, particularly if the conditions to trigger the HL transition occur very rarely

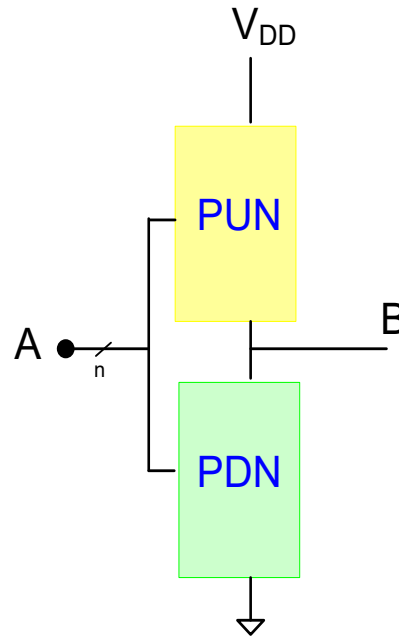
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Dynamic Logic



- PTL reduced complexity of either PUN or PDN to single “resistor”
- PTL relaxed requirement of all n-channel or all p-channel devices in PUN/PDN



What is the biggest contributor to area?

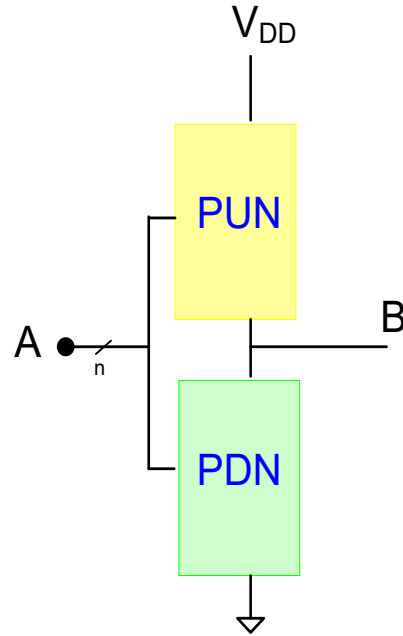
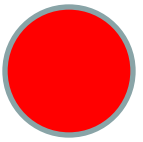
PUN (3X active area for inverter, more for NOR gates, and Well)

What is biggest contributor to dynamic power dissipation ?

PUN and is responsible for approximately 75% of the dynamic power dissipation in equal rise/fall inverter, and much more in NOR gates !

Can the PUN be eliminated W/O compromising signal levels and power dissipation?

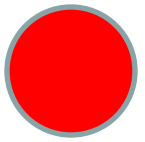
Dynamic Logic



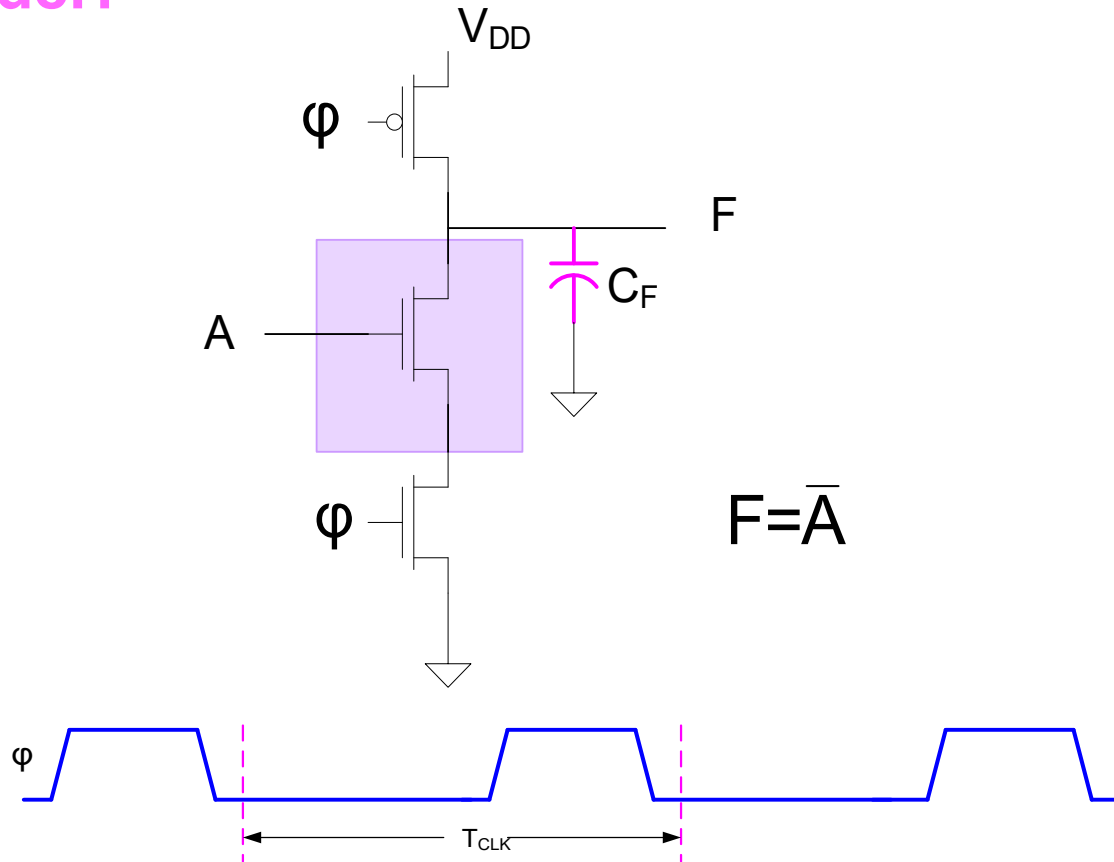
Can the PUN be eliminated W/O compromising signal levels and power dissipation?

Benefits could be most significant !

Dynamic Logic



Consider:

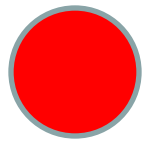


Precharges C_F to “1” when ϕ is low

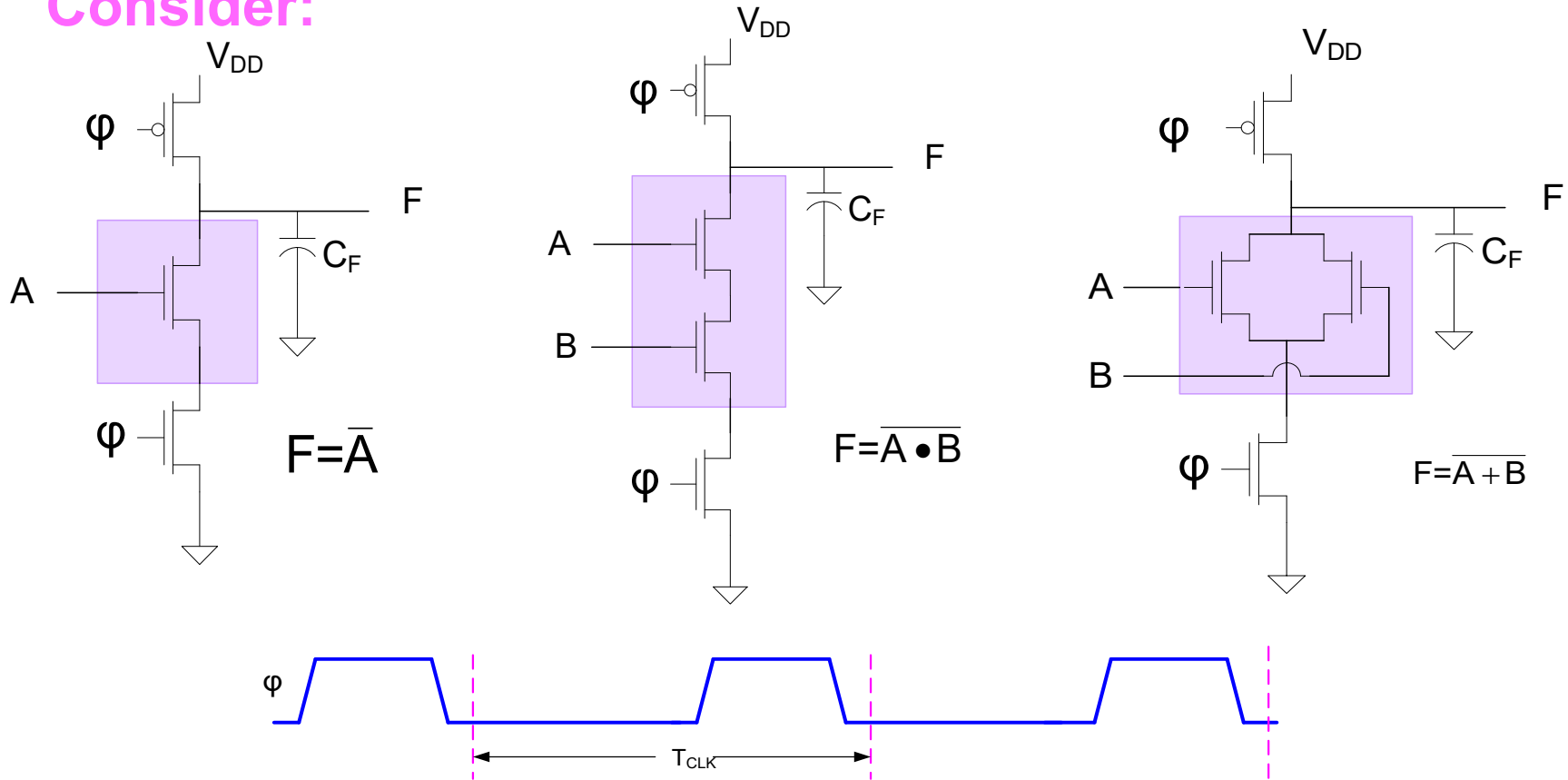
F either stays high if output is to be high or changes to low on evaluation

C_F is usually the parasitic capacitances on the node (drain diffusion and gates)

Dynamic Logic

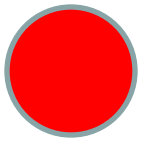


Consider:

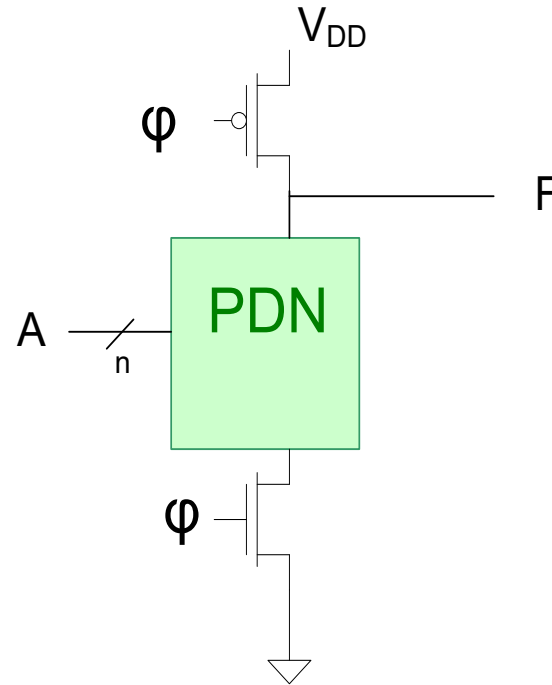


- **Termed Dynamic Logic Gates**
- **Parasitic capacitors actually replace C_F**
- **If Logic Block is n-channel, will have rail to rail swings**
- **Logic Block is simply a PDN that implements \overline{F}**

Dynamic Logic



Basic Dynamic Logic Gate

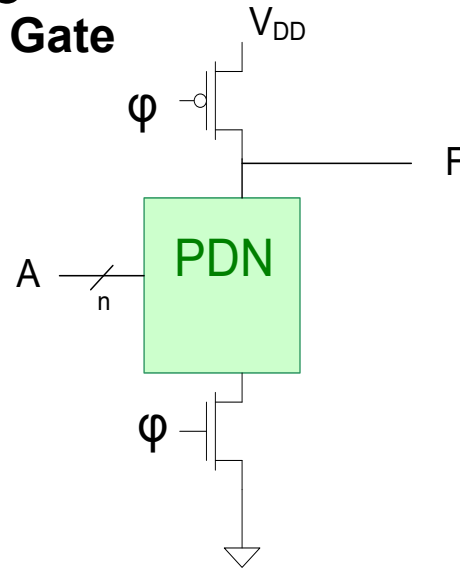


Any of the PDNs used in complex logic gates would work here !

- Have eliminate the PUN !
- Ideally will have a factor of 4 or more reduction in C_{IN}
- Ideally will have a factor of 4 or more reduction in dynamic power dissipation relative to that of equal rise/fall !
- Ideally will have a factor of 2 reduction in dynamic power dissipation relative to that of minimum size!

Dynamic Logic

Basic Dynamic Logic Gate



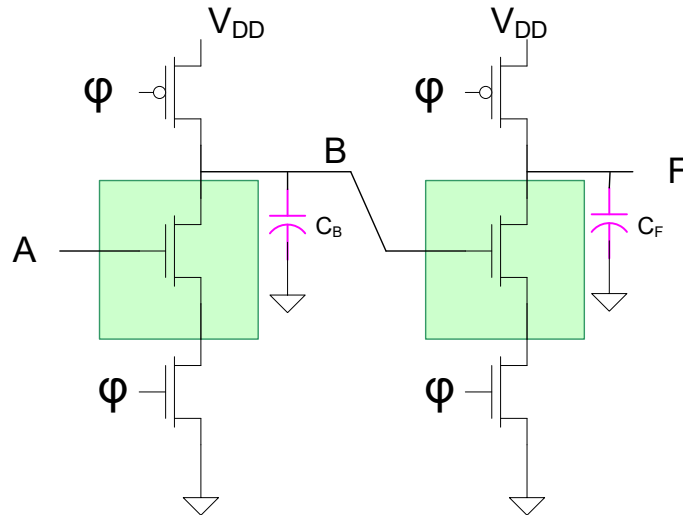
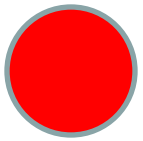
Advantages:

- Lower dynamic power dissipation (Ideally 4X)
- Improved speed (ideally 4X)

Limitations:

- Output only valid during evaluate state
- Need to route a clock
(and this dissipates some power)
- Premature Discharge !
- More complicated
- Charge storage on internal nodes of PDN
- No Static hold if output H
- Dynamic power dissipation in pre-charge circuit

Dynamic Logic



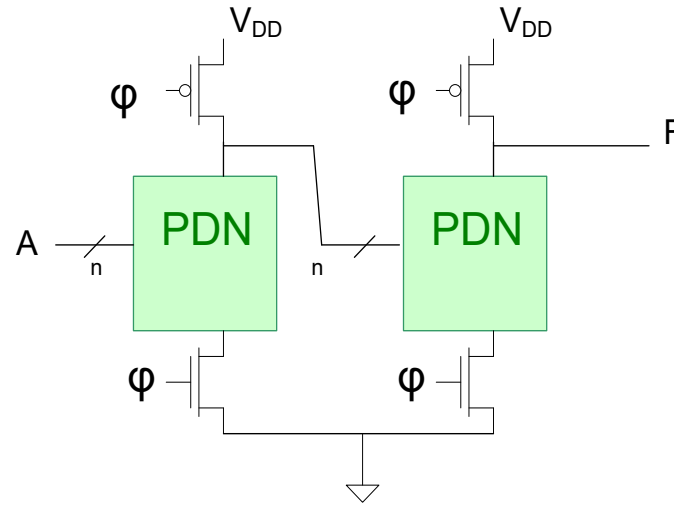
Premature Discharge Problem

B will be pulled high during the pre-charge state and try to discharge C_F thus pulling F low

If input A is high, then if F goes low at the start of the evaluate cycle, there is no way to recover a high output later in the evaluate phase - i.e. there may be a boolean error!.

Can not reliably cascade dynamic logic gates !

Dynamic Logic



Premature Discharge Problem

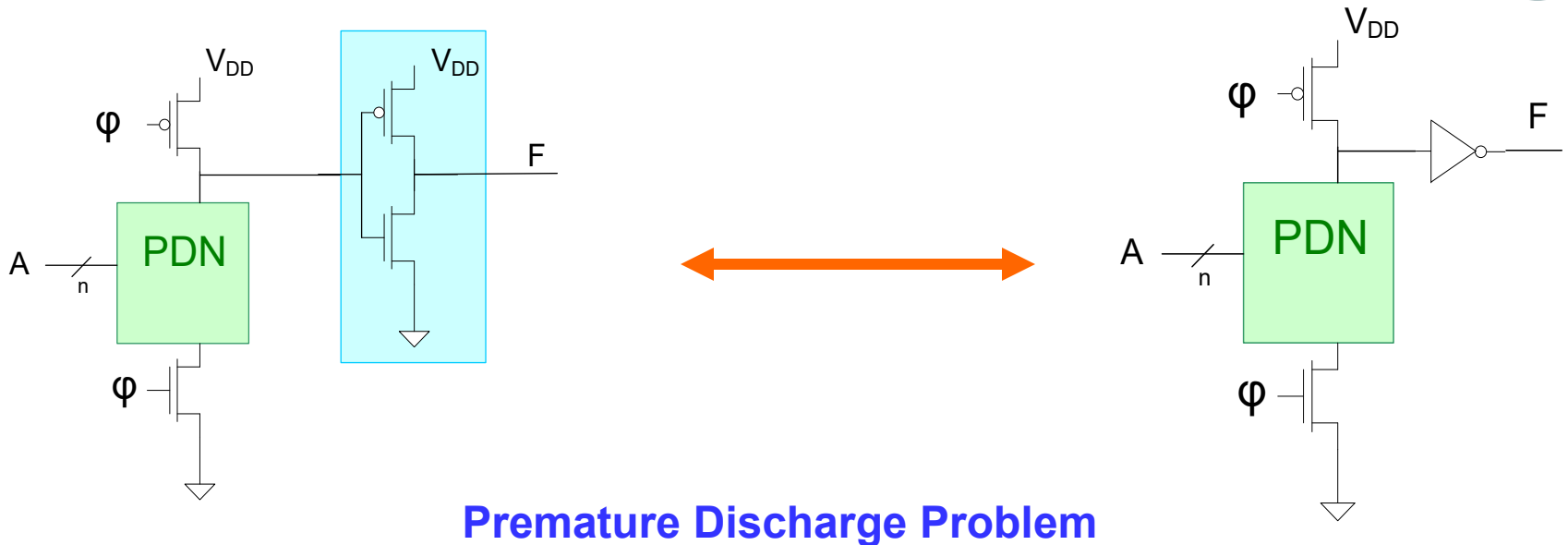
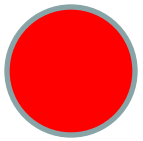
This problem occurs when any inputs to an arbitrary dynamic logic gate create an R_{PD} path in the PDN during at the start of the evaluate phase that is not to pull down later in that evaluate phase

How can this problem be fixed?

Precharging to the low level all inputs to a PDN that may change to the high state later in the evaluate cycle (called domino)

Alternating gates with n-channel and p-channel pull networks (Zipper Logic)

Dynamic Logic



Adding an inverter at the output will cause F to precharge low so it can serve as input to subsequent gate w/o causing premature discharge

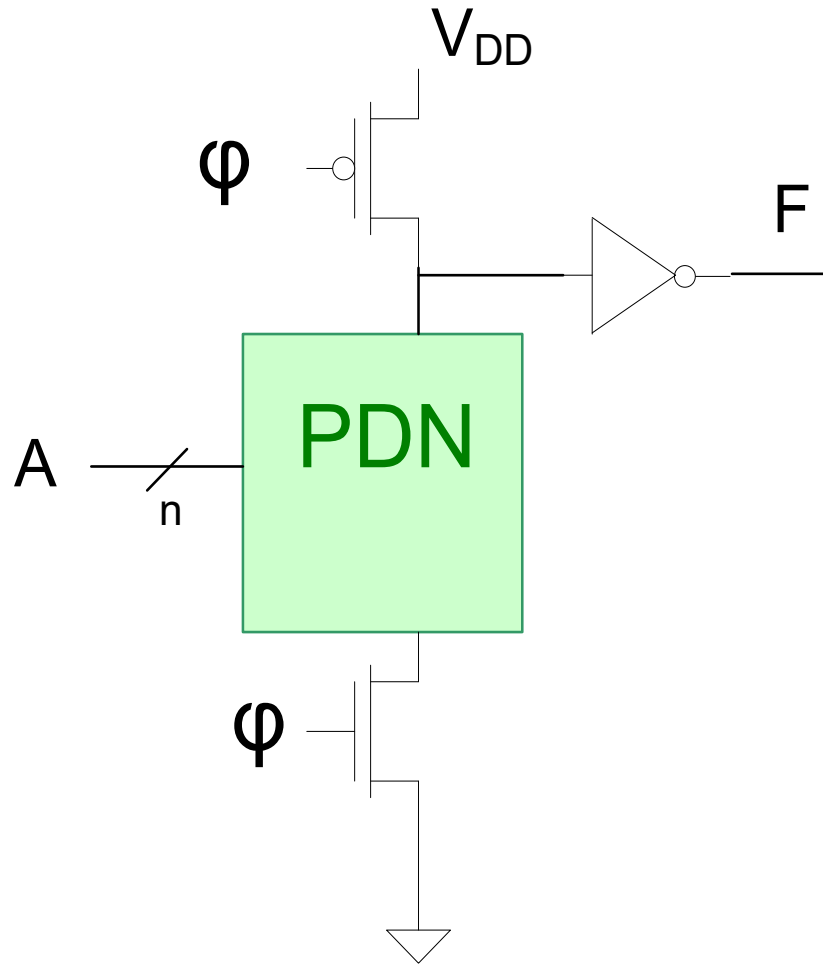
Implement F instead of \bar{F} in the PDN

Termed **Domino Logic**

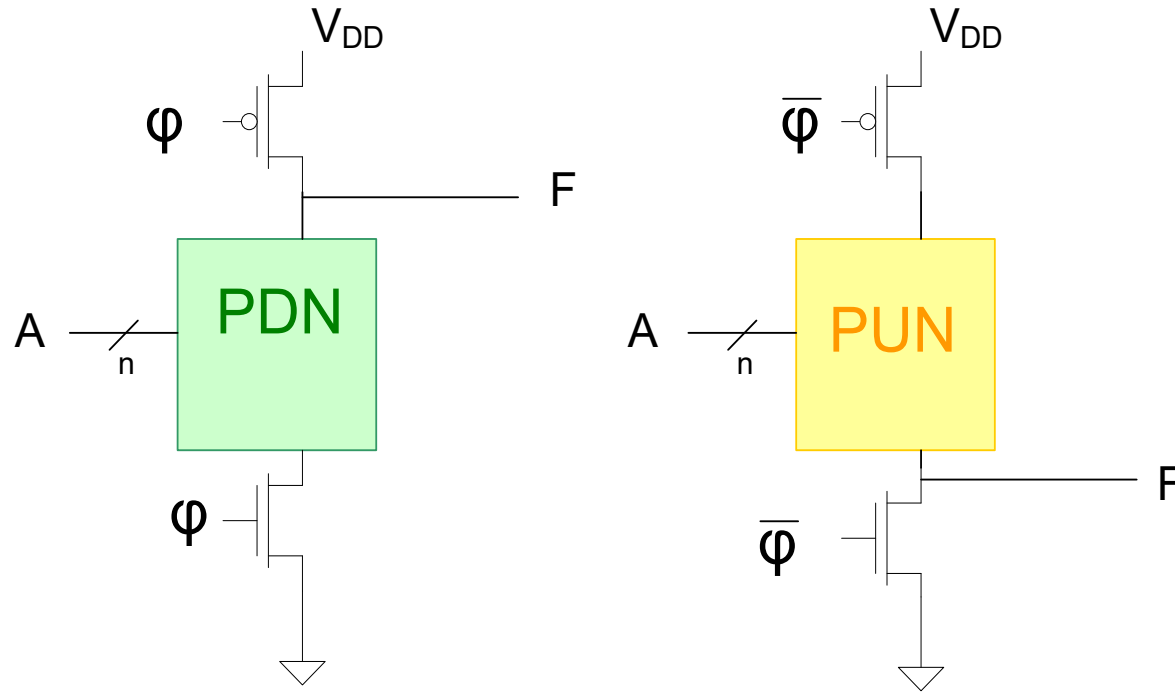
Some additional dynamic power dissipation in the inverter

Some additional delay during the evaluate state in inverter

Domino Logic

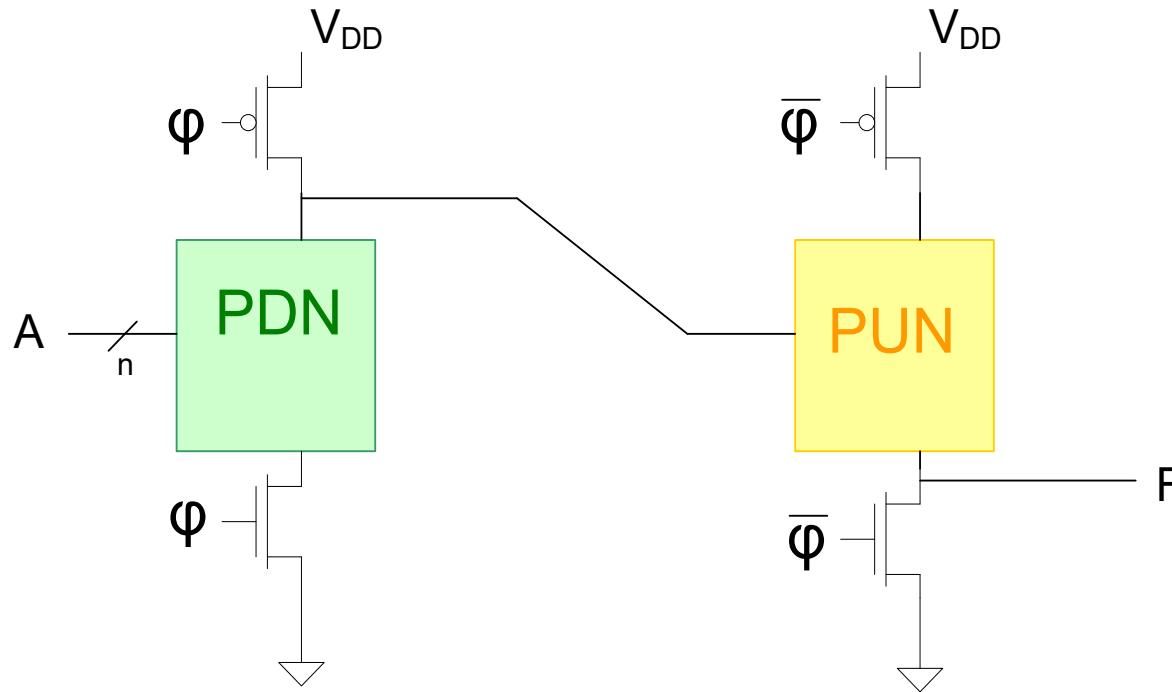
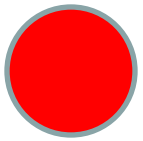


Dynamic Logic



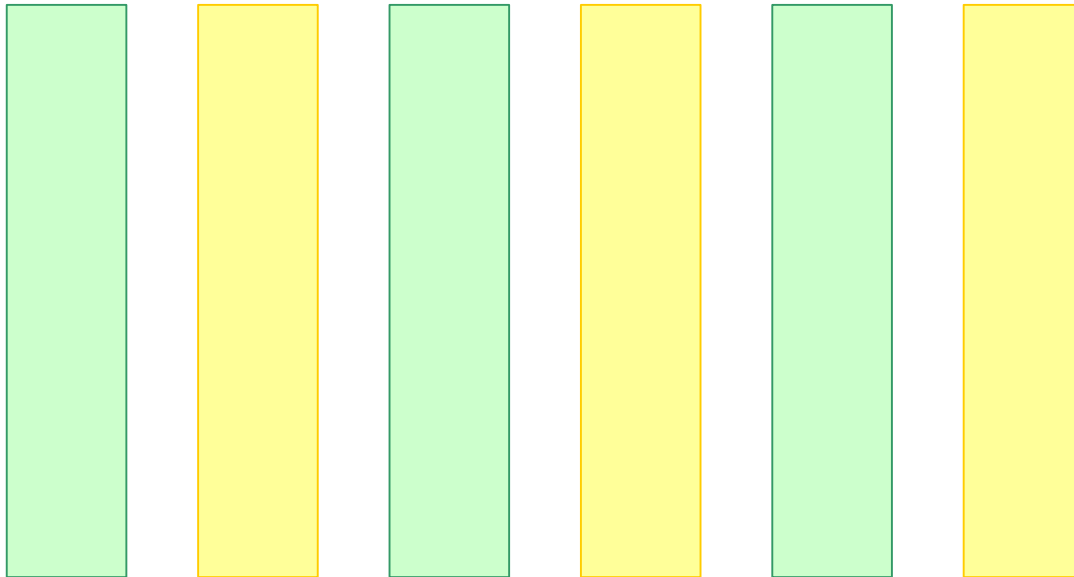
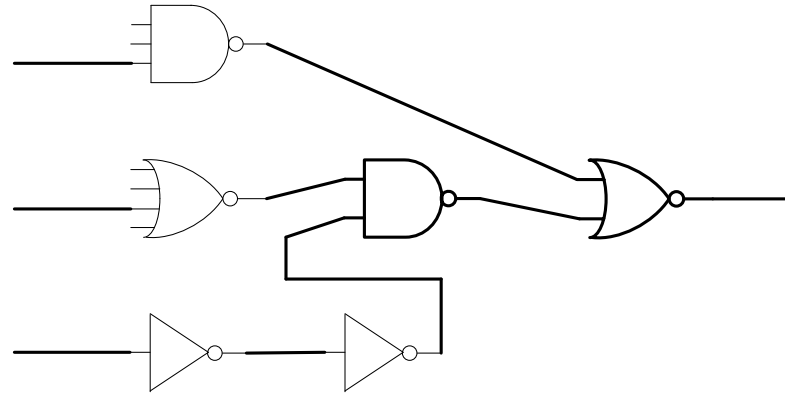
- p-channel logic gate will pre-charge low
- Phasing of PUN and PDN networks is reversed
- Some performance loss with p-channel logic devices
- Direct coupling between alternate type dynamic gates is possible without causing a premature discharge problem

Dynamic Logic



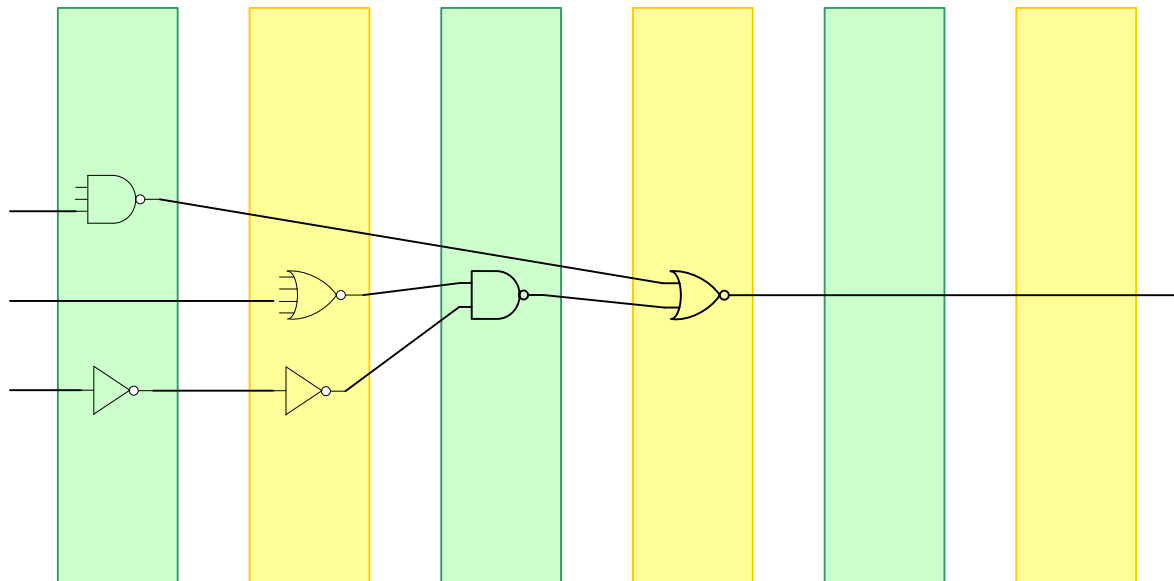
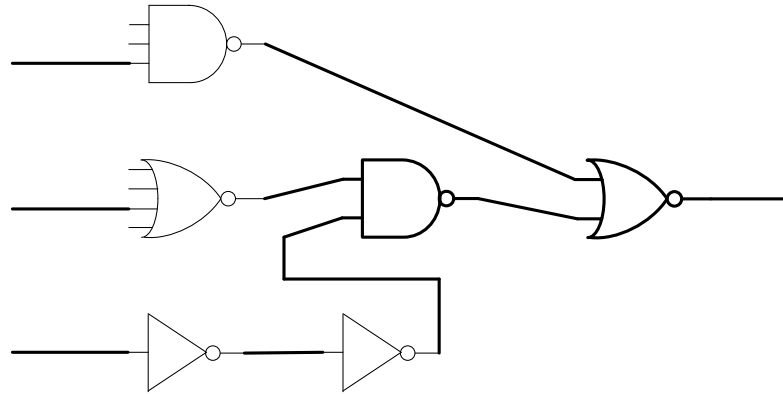
Direct coupling between alternate type dynamic gates

Zipper Logic



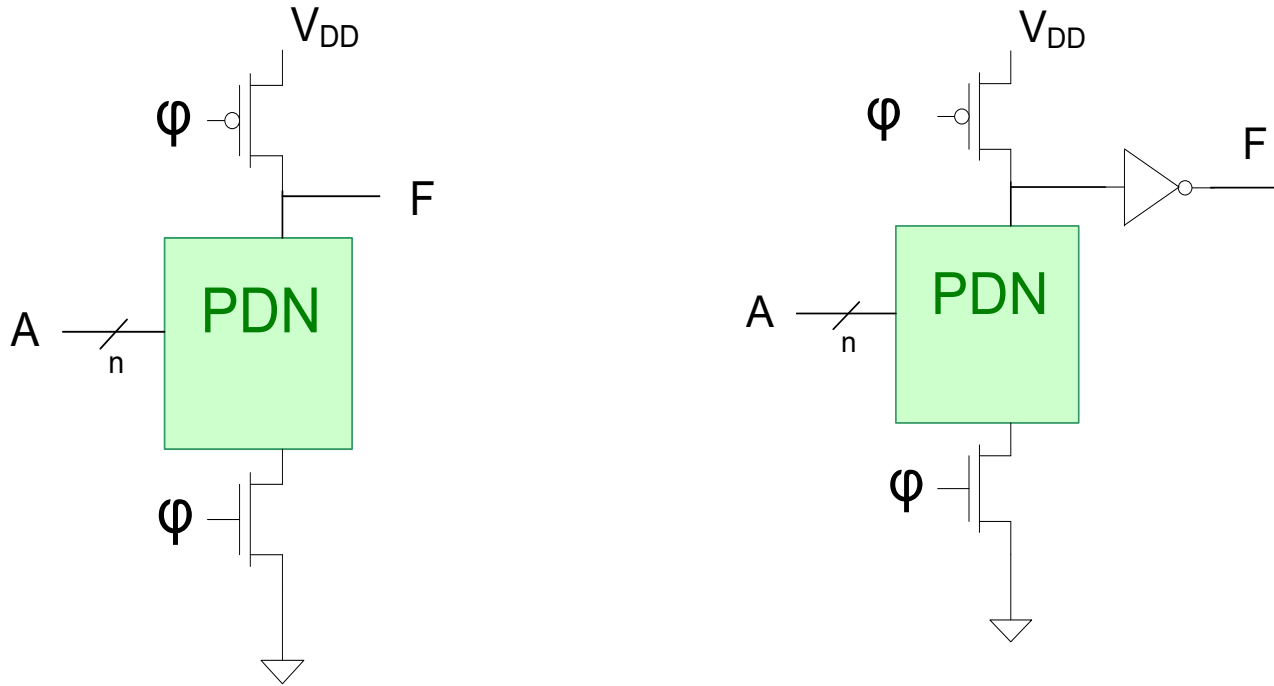
Map gates to appropriate precharge type

Zipper Logic



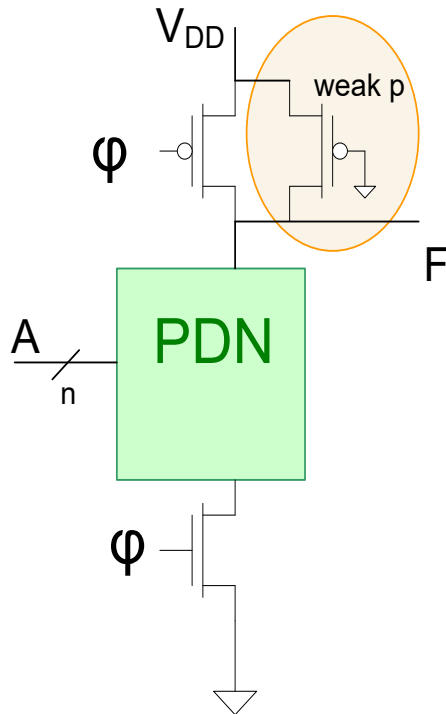
Acceptable Implementation in Zipper

Static Hold Option

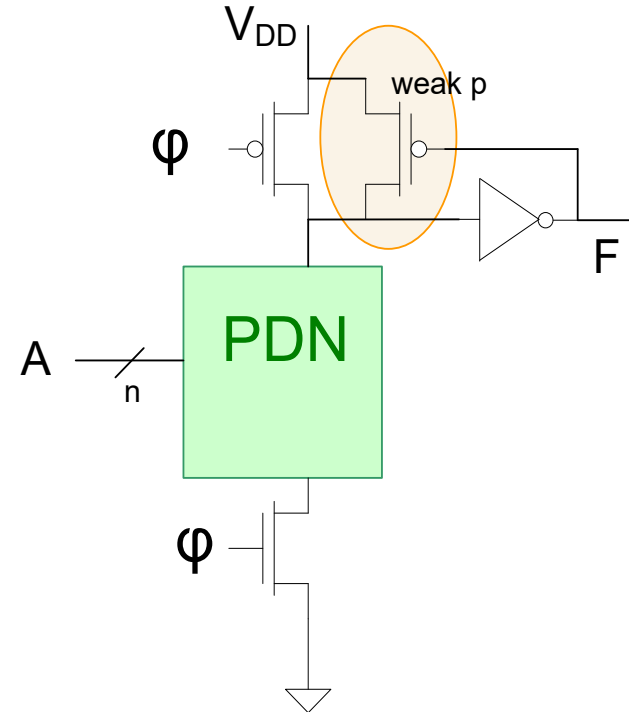


If not clocked, charge on upper node of PDN will drain off causing H output to degrade

Static Hold Option

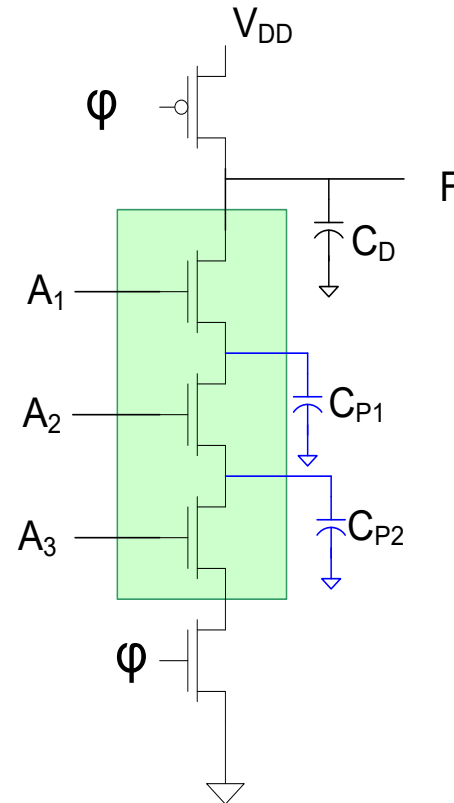


- weak p will hold charge
- size may be big (long L)
- some static power dissipation
- can use small current source
- sometimes termed “keeper”



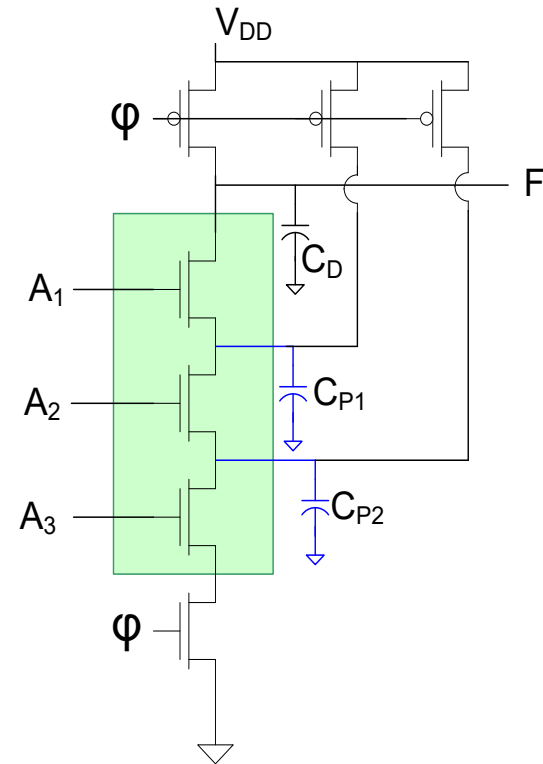
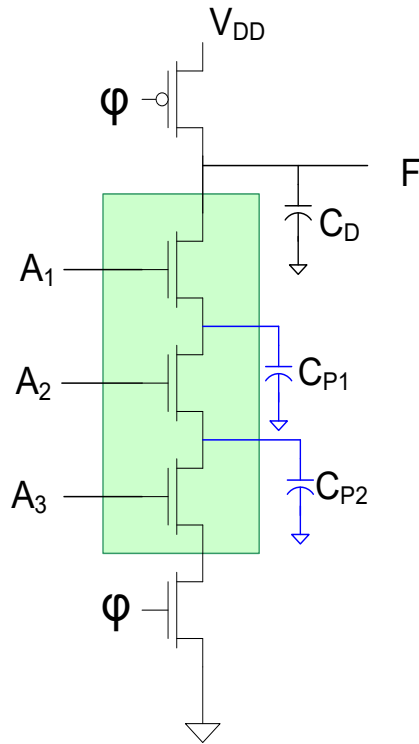
- weak p will hold charge
- size may be big (long L)
- can eliminate static power with domino
- sometimes termed “keeper”

Charge stored on internal nodes of PDN



If voltage on C_{P1} and C_{P2} was 0V on last evaluation, these may drain charge (charge redistribution) on C_P if output is to evaluate high (e.g. On last evaluation $A_1=A_2=A_3=H$, on next evaluation $A_3=L$, $A_1=A_2=H$.)

Charge stored on internal nodes of PDN



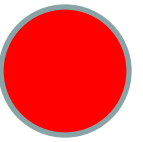
Can precharge internal nodes to eliminate undesired charge redistribution

Dynamic Logic

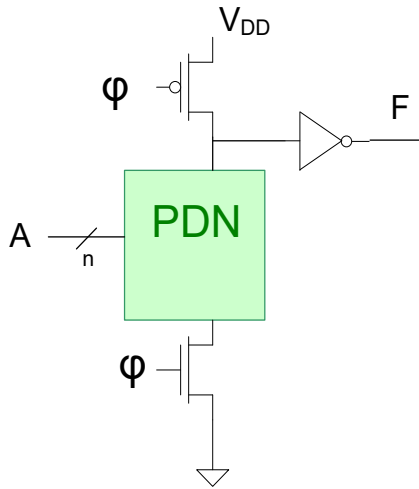
Many variants of dynamic logic are around

- Domino
- Zipper
- Ratio-less 2-phase
- Ratio-less 4-phase
- Output Prediction Logic
- Fully differential

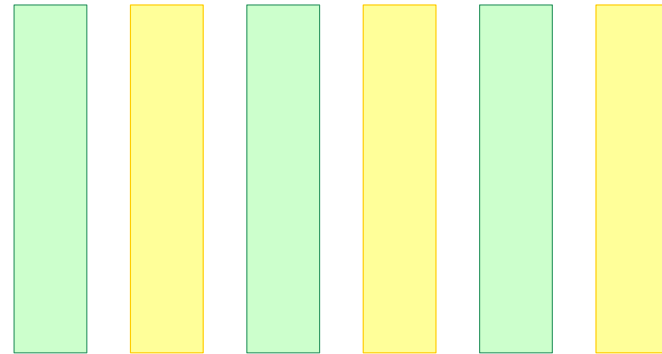
Benefits disappear, however, when interconnect (and diffusion) capacitances dominate gate capacitances



Future of Dynamic Logic



Domino



Zipper

Dynamic logic will likely disappear in deep sub-micron processes because interconnect parasitics will dominate gate parasitics

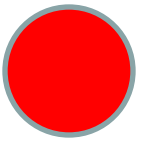
Other types of Logic (list is not complete and some have many sub-types)

From Wikipedia:

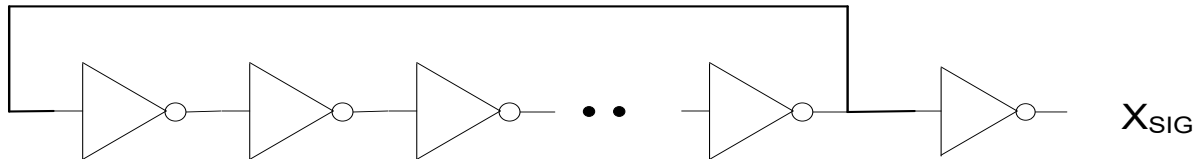
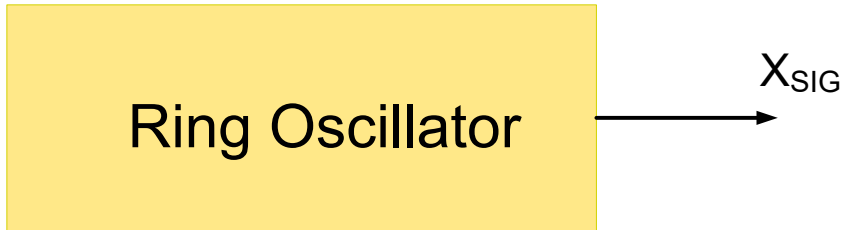
- B**
 - [BiCMOS](#)
- C**
 - [CMOS](#)
 - [Cascode Voltage Switch Logic](#)
 - [Clocked logic](#)
 - [Complementary Pass-transistor Logic](#)
 - [Current mode logic](#)
 - [Current steering logic](#)
- D**
 - [Differential TTL](#)
 - [Diode logic](#)
 - [Diode–transistor logic](#)
 - [Domino logic](#)
 - [Dynamic logic \(digital logic\)](#)
- E**
 - [Emitter-coupled logic](#)
- F**
 - [Four-phase logic](#)
- G**
 - [Gunning Transceiver Logic](#)
- H**
 - [HMOS](#)
 - [HVDS](#)
 - [High-voltage differential signaling](#)
- I**
 - [Integrated injection logic](#)
- L**
 - [LVDS](#)
 - [Low-voltage differential signaling](#)
 - [Low-voltage positive emitter-coupled logic](#)
- M**
 - [Multi-threshold CMOS](#)
- N**
 - [NMOS logic](#)
- P**
 - [PMOS logic](#)
 - [Philips NORbits](#)
 - [Positive emitter-coupled logic](#)
- R**
 - [Resistor-transistor logic](#)
- S**
 - [Static logic \(digital logic\)](#)
- T**
 - [Transistor–transistor logic](#)

Digital Building Blocks

- Shift Registers
- Sequential Logic
- Shift Registers (stack)
- Array Logic
- Memory Arrays



Ring Oscillators



- **Odd number of stages will oscillate (even will not oscillate)**
- **Waveform nearly a square wave if n (number of stages) is large**
- **Output will slightly imbalance ring and device sizes can be compensated if desired**
- **Usually use a prime number (e.g. 31)**
- **Number of stages usually less than 50 (follow by dividers)**
- **Frequency highly sensitive to process variations and temperature**

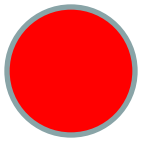
$$f_{OSC} \cong \frac{1}{nt_{PROP}}$$

- **n is the number of stages**
- **t_{PROP} is the propagation delay of a single stage (all assumed identical)**

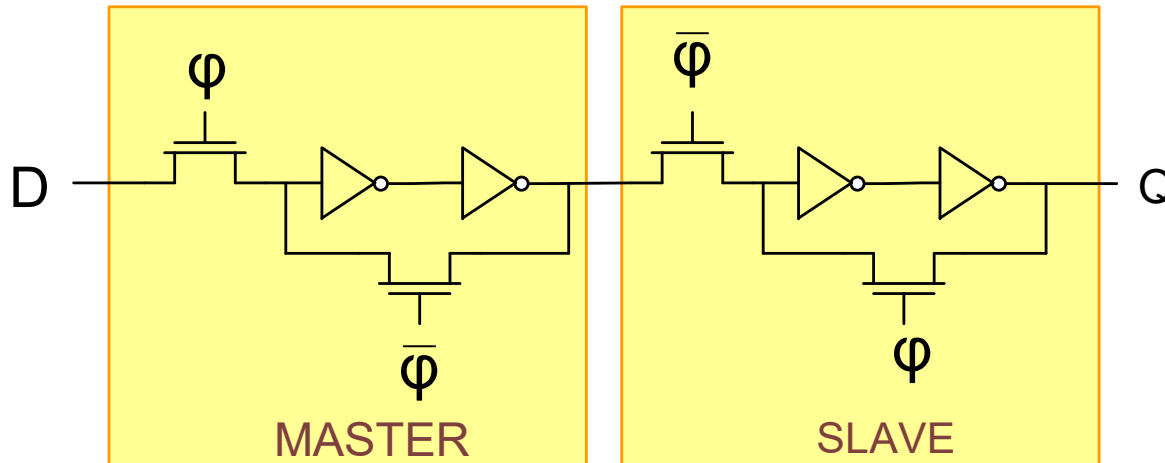
Sequential Logic Circuits

- **Flip Flops needed for sequential logic circuit**
- **Only one type of flip flop is required**
- **Invariably require clocked edge-triggered master-slave flop flops**
- **Flip flop circuits can be very simple**
- **Flip flops are part of Standard Cell Libraries**

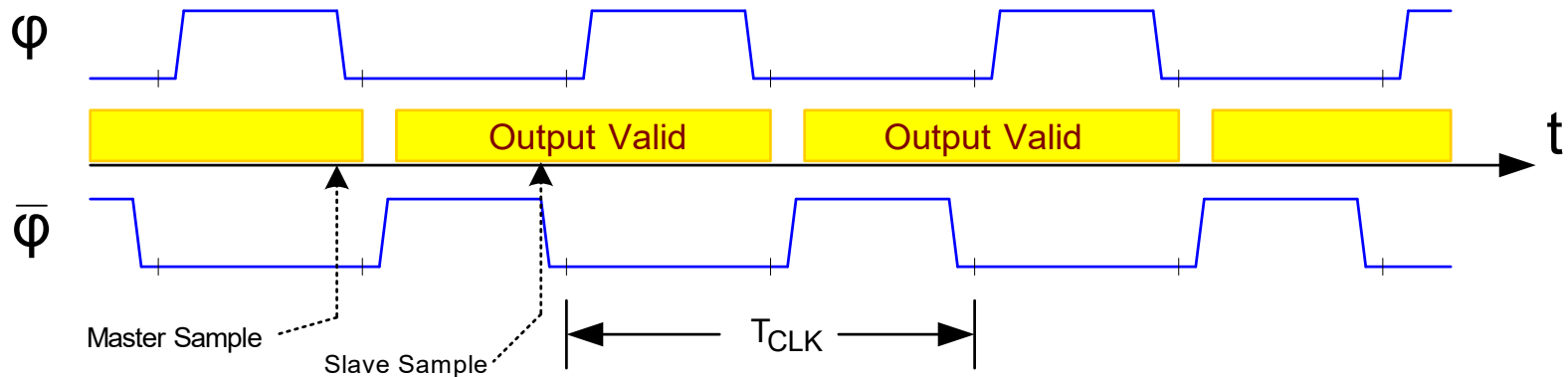
Flip Flops



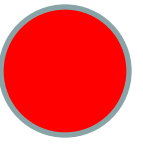
Master-Slave Edge-triggered D Flip Flop



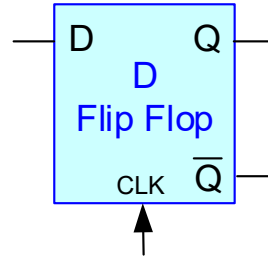
Timing Diagram



- 12 transistors (but will work with 10)
- Many other simple D Flip-flops exist as well

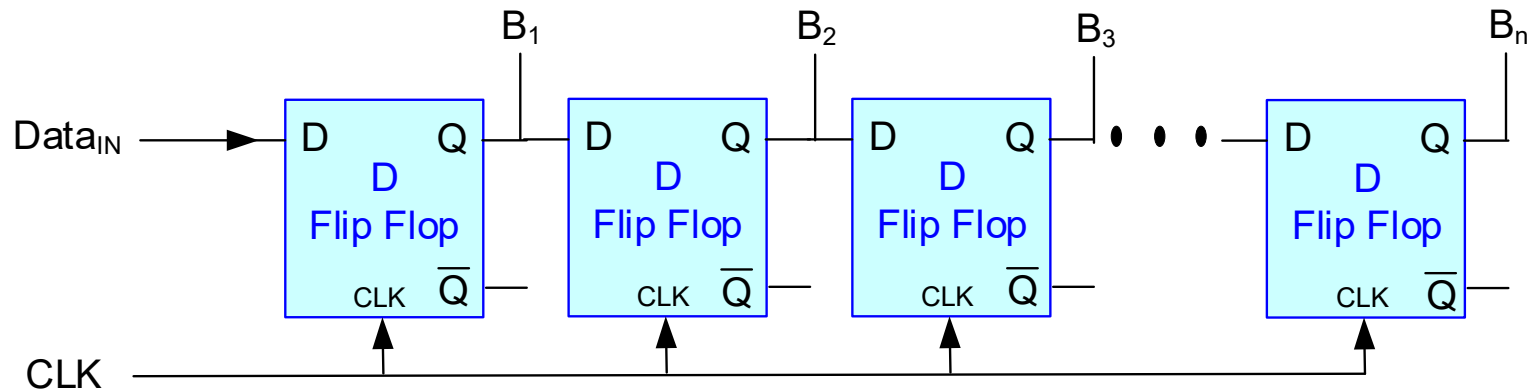


Shift Registers



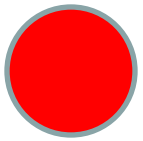
Edge-triggered Master-Slave D Flip Flop

Basic Edge-Triggered Shift Register

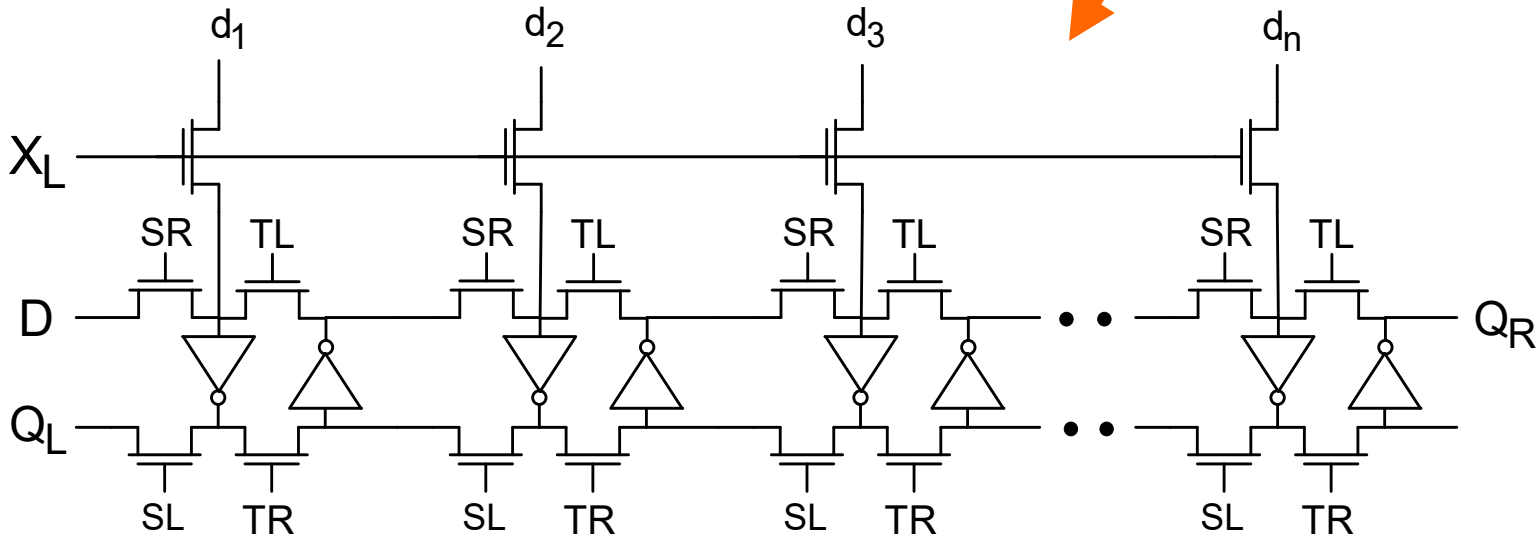
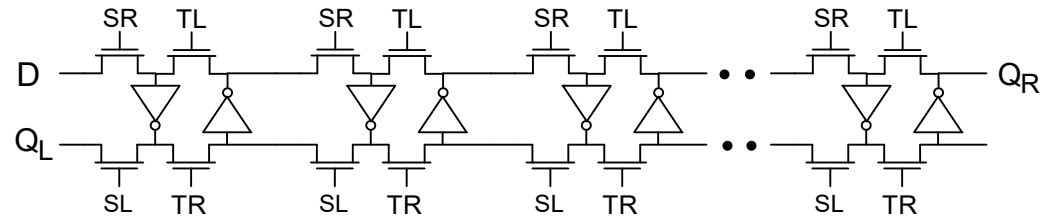


- **Can be easily modified for parallel load**
- **Can be easily modified for parallel-serial and serial-parallel conversion**

Shift Registers



Dynamic Shift Register



n-bit Parallel-Load, Parallel-Read Bidirectional Dynamic Shift Register

- Useful for Parallel to Serial and Serial to Parallel Conversion
- Can be put in static hold state if T_L and T_R replaced with $H \nabla TL$ and $H \nabla TL$

Array Logic

- Array logic is often used for sections of logic that may change later in the design or that will be changed for different variants of a product
- FPGA are a special case of array logic
- Can personalize array logic with only one layer of metal
 - Very quick turn-around and low incremental costs (as few as one additional mask)

Array Logic

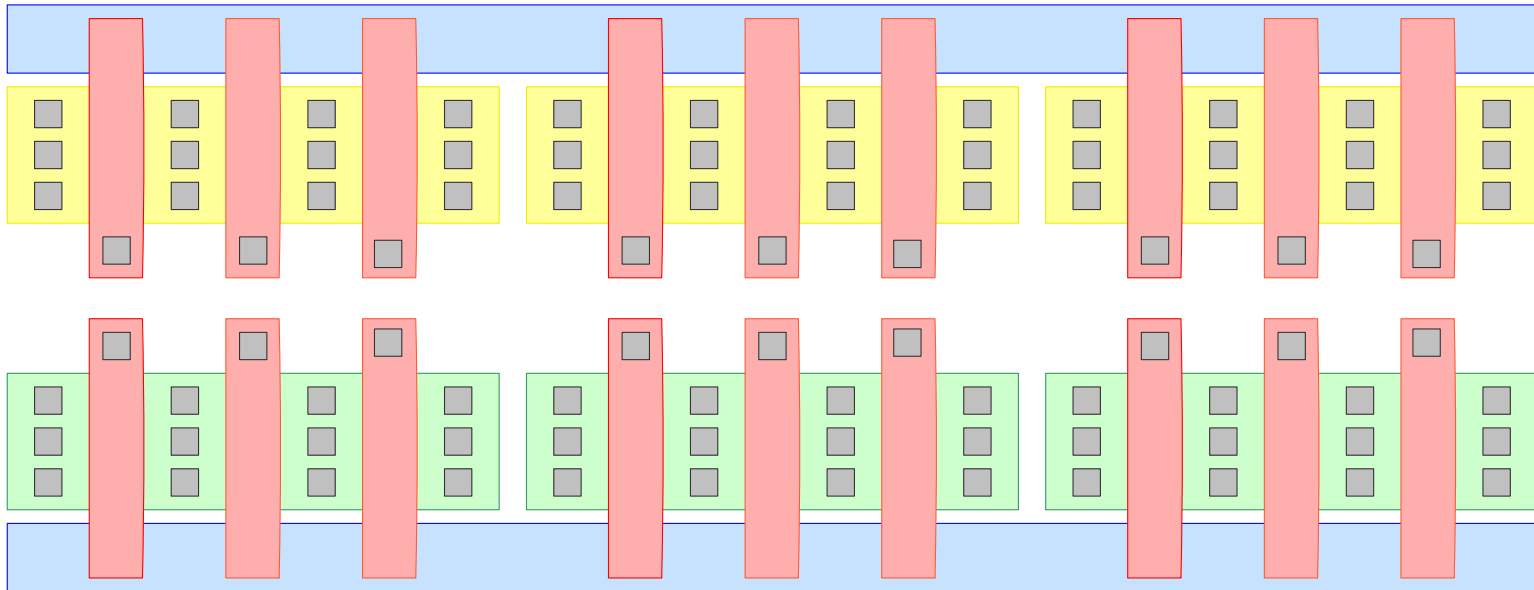
Will consider only two types

- Gate Array
- Sea of Gates

Variants of the following approach are possible depending upon process but this will convey the basic concepts

Array Logic

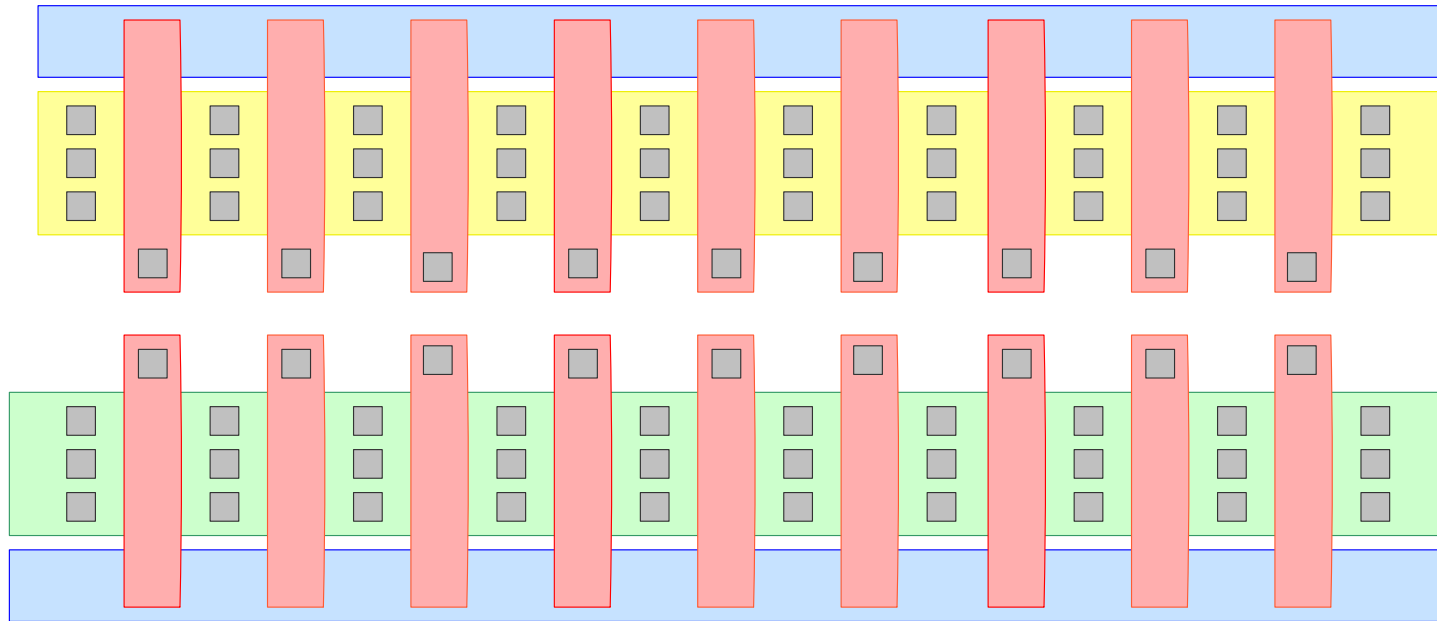
Gate Array



- Can add M1 (blue), M2 (purple), contact (M1 to Poly), via (M1 to M2) (3 simple masks)
- Upper and lower metal shown actually lie above poly and are automatically present
- Assume upper M1 is V_{DD} and lower M1 is V_{SS}
- Array can be very large
- Routing channels between segments of array

Array Logic

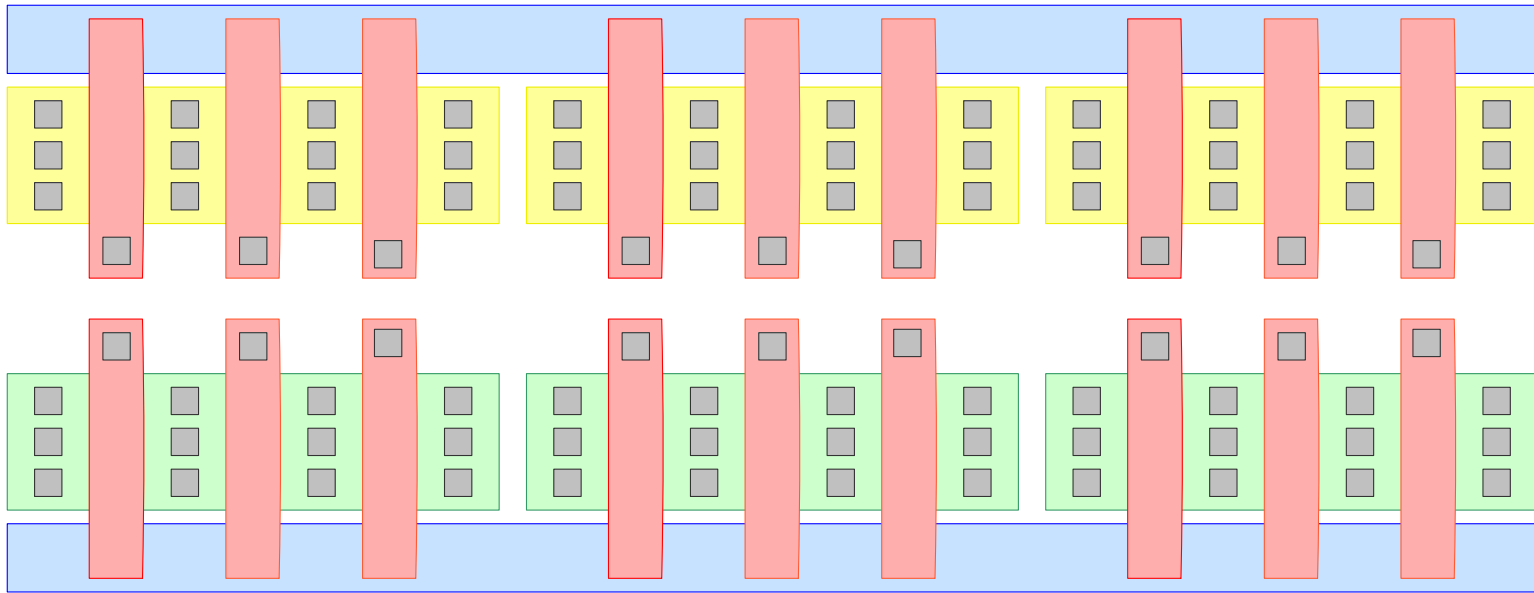
Sea of Gates



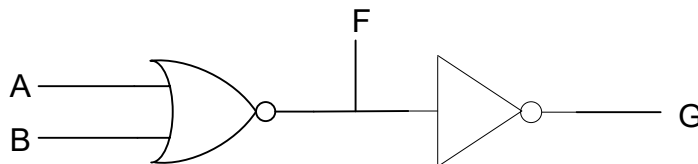
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- Routing channels between segments of array

Array Logic

Gate Array



Example:

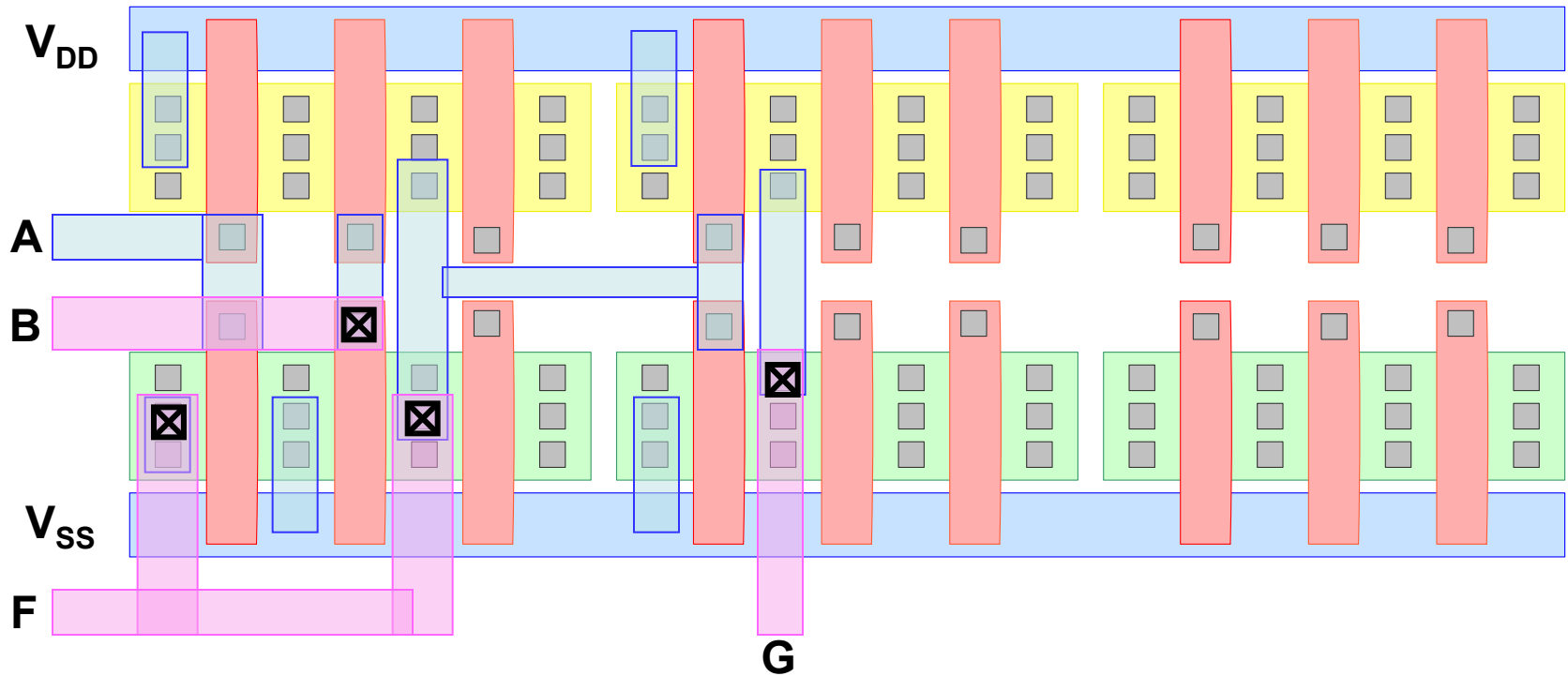


⊠ Via (M1 to M2)

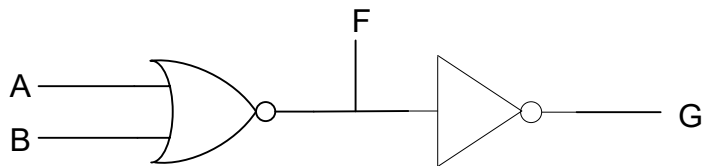
■ Contact (M1 to diff, Poly)

Array Logic

Gate Array



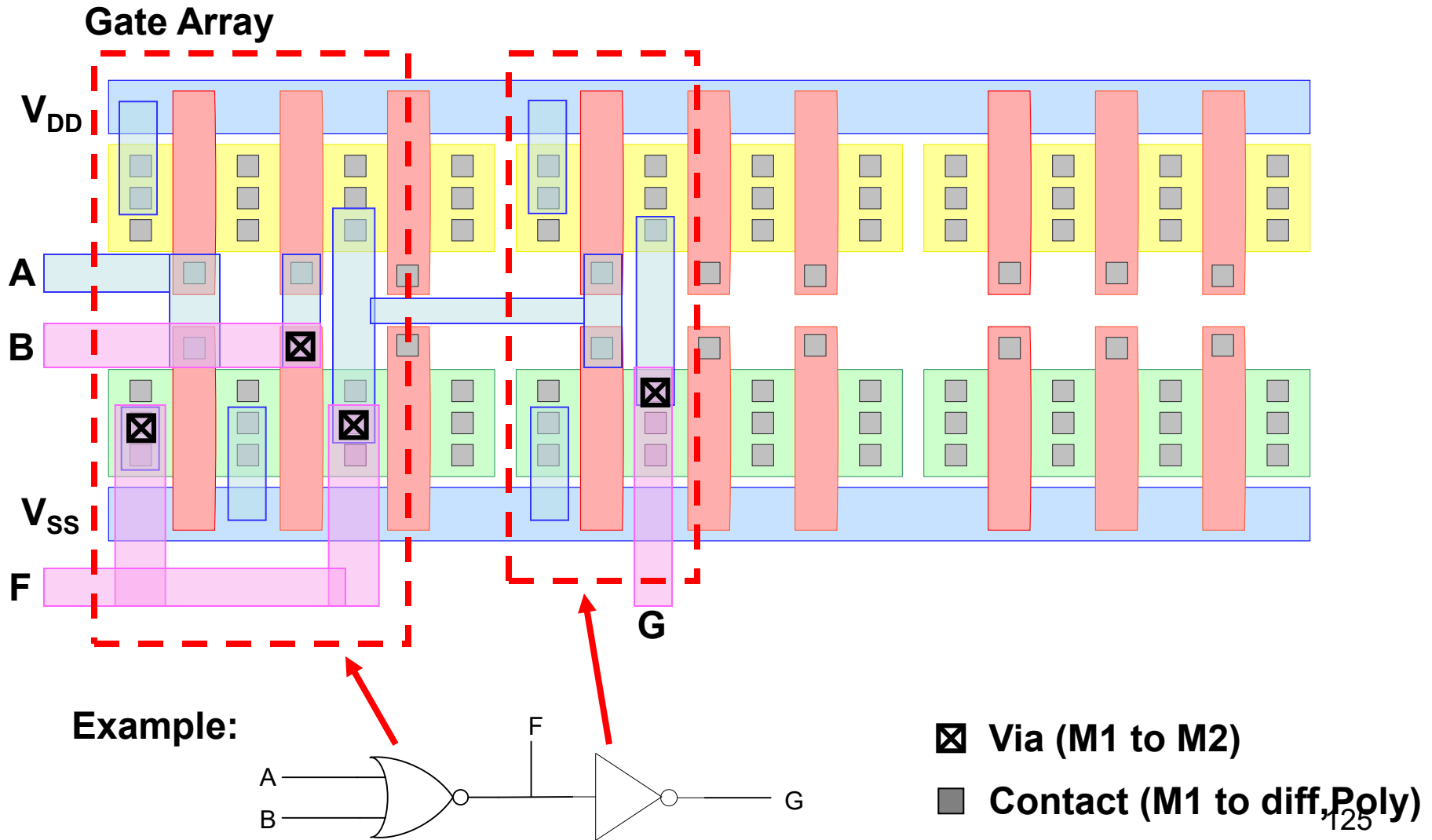
Example:



⊗ Via (M1 to M2)

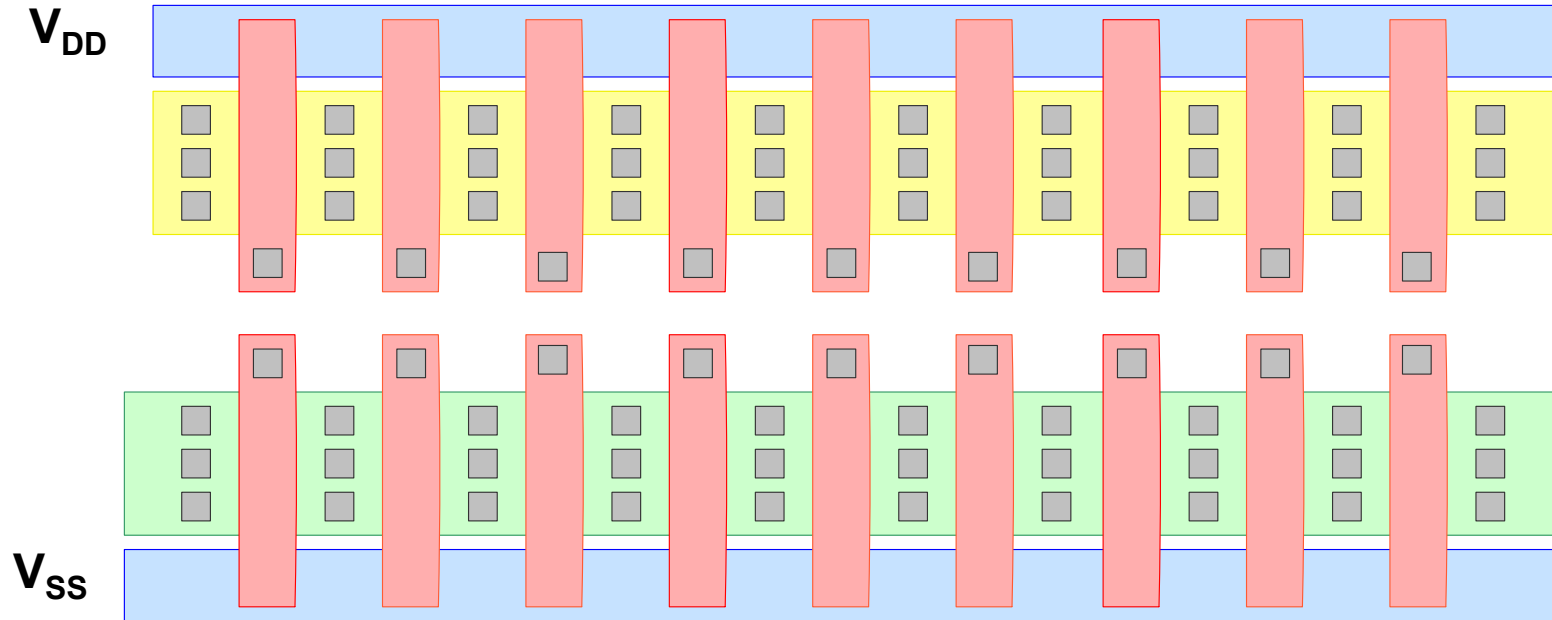
■ Contact (M1 to diff, Poly)

Array Logic

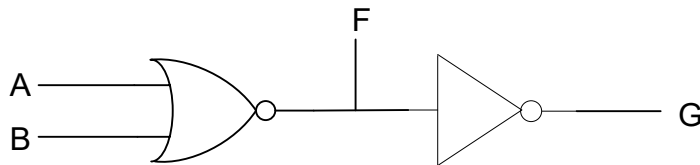


Array Logic

Sea of Gates



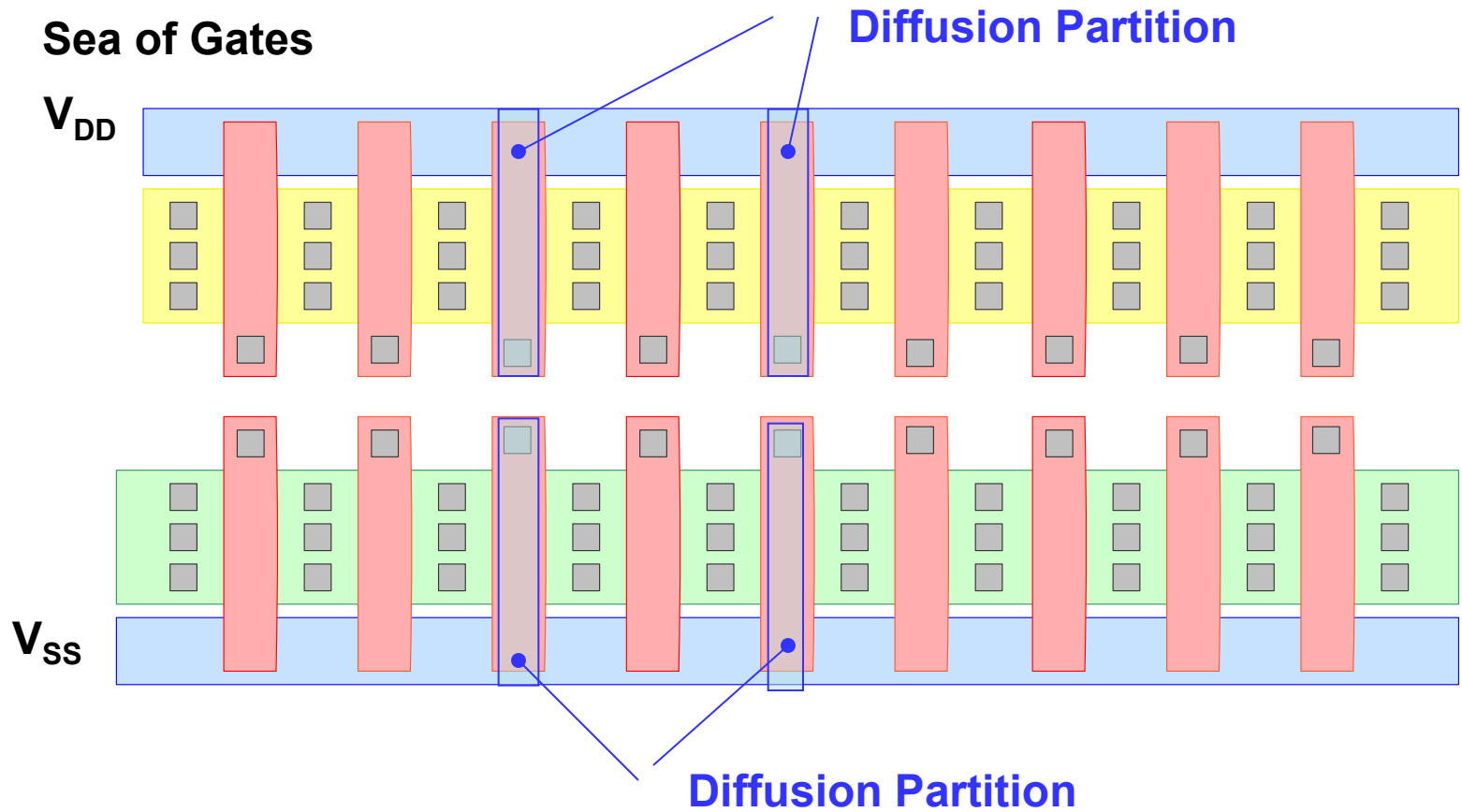
Example:



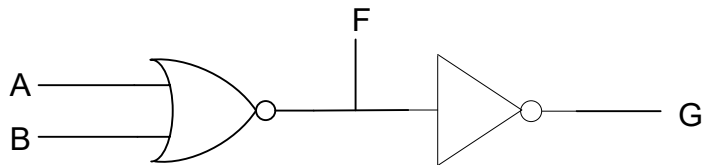
⊠ Via (M1 to M2)

■ Contact (M1 to diff, Poly)

Array Logic



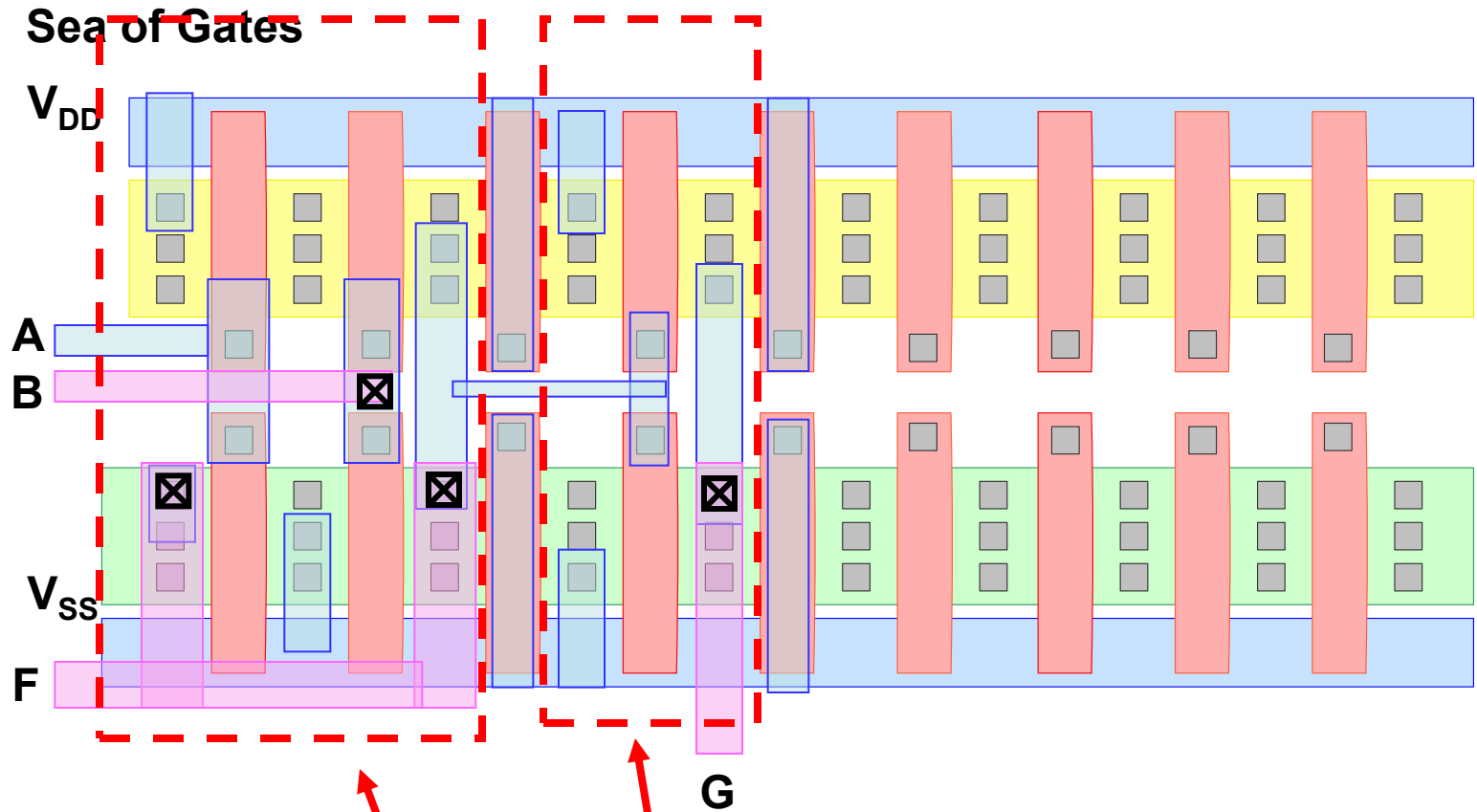
Example:



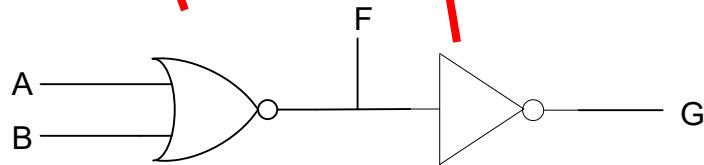
☒ Via (M1 to M2)

■ Contact (M1 to diff, Poly)

Array Logic



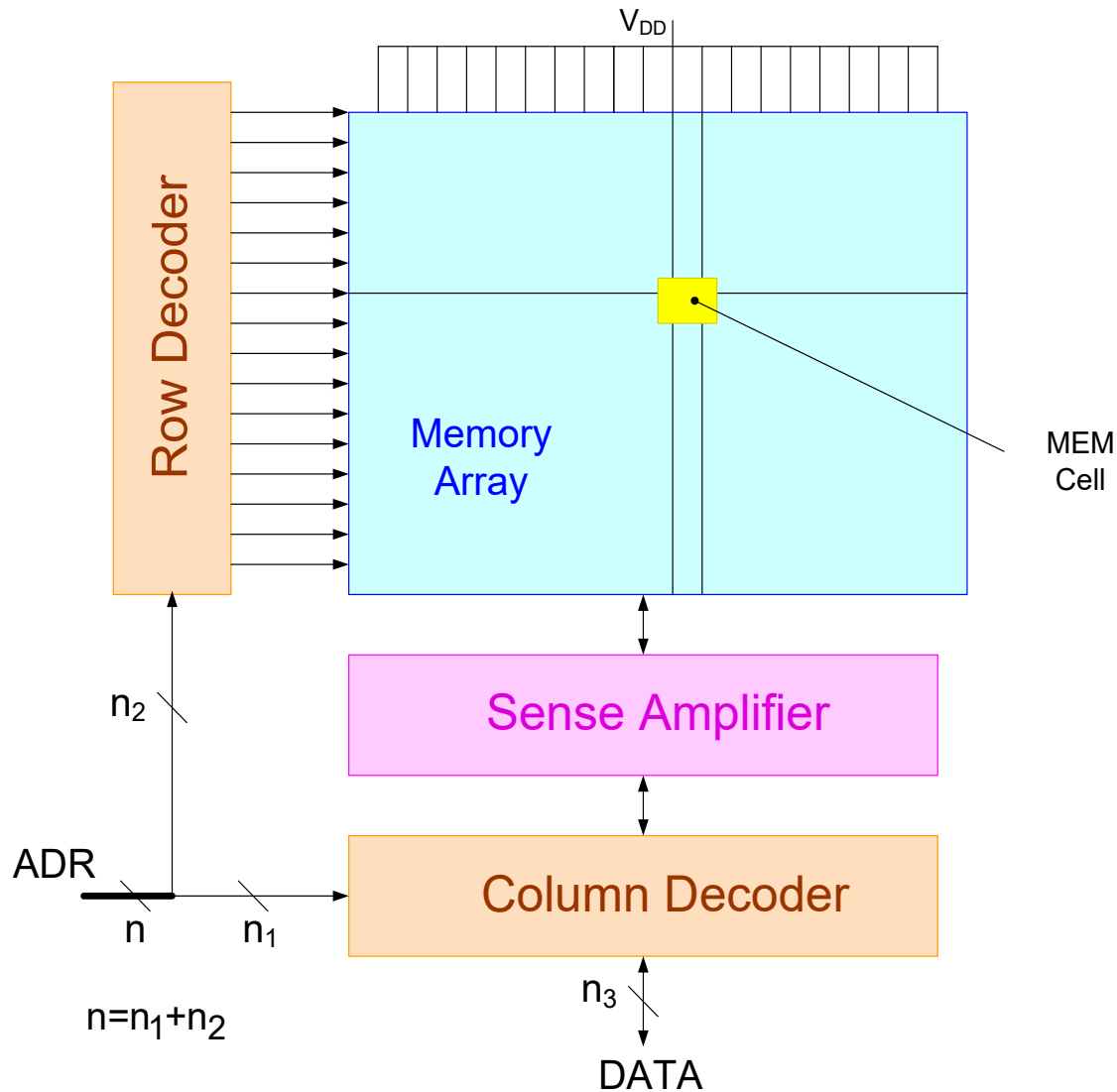
Example:



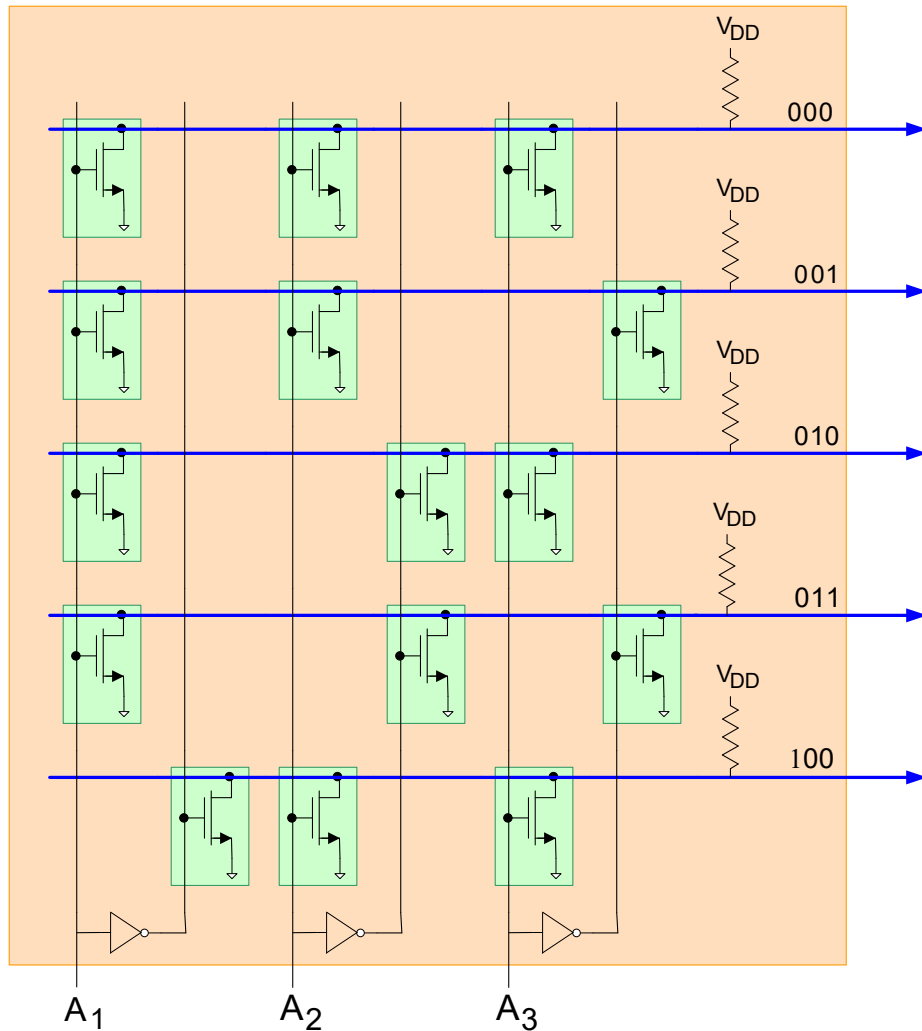
⊠ Via (M1 to M2)

■ Contact (M1 to diff, Poly)

Typical Memory Structure



Row Decoder Architectures



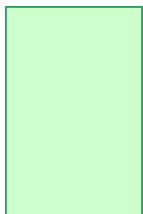
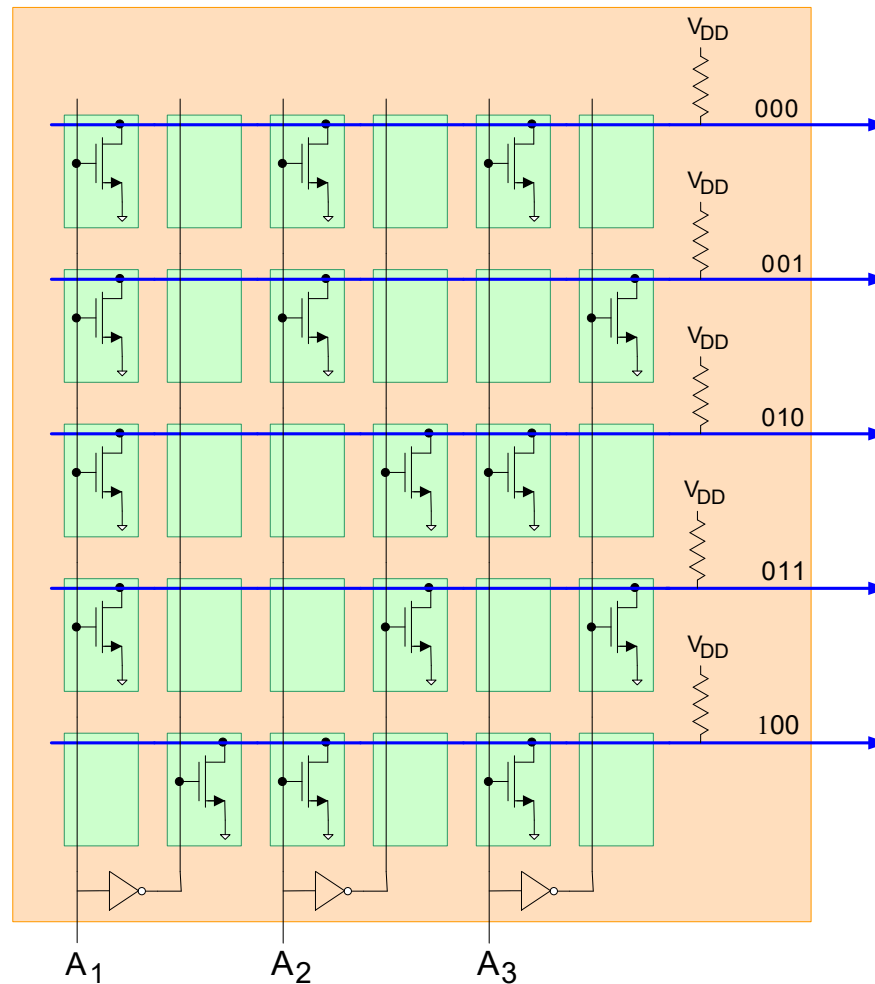
$$R_k = \bar{A}_1 \cdot \bar{A}_2 \cdot \bar{A}_3$$

$$R_k = \overline{(A_1 + A_2 + A_3)}$$

Row decoder is Pseudo
n-MOS NOR Gate

Typically $n/2$ inputs where n is the
address length

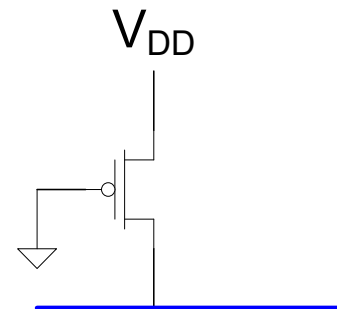
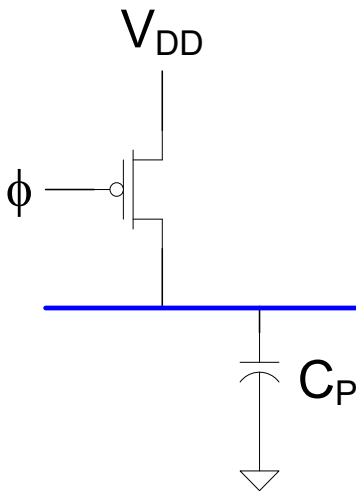
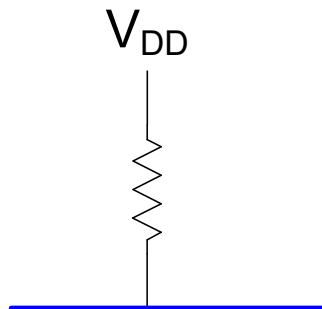
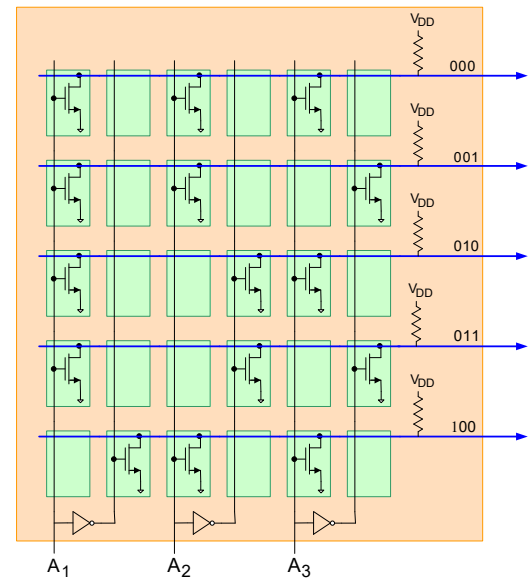
Row Decoder Architectures



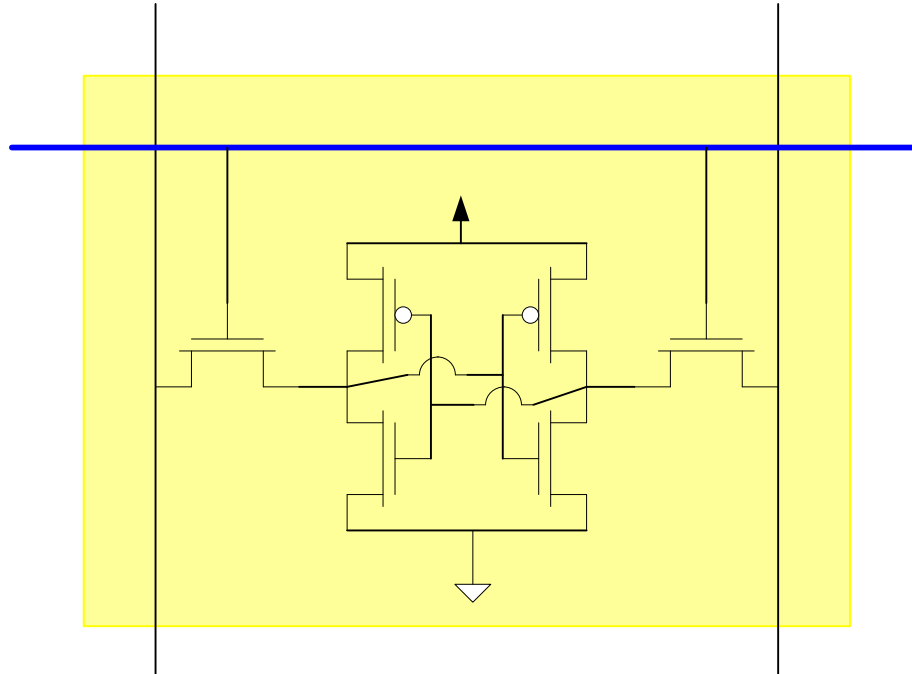
Transistor sites typically reserved in the layout for efficient, compact layout

Row Decoder Architectures

Pull-up resistor implemented with either weak p or with dynamic precharge by taking clock ϕ low to precharge to high (thus dynamic NOR gate)



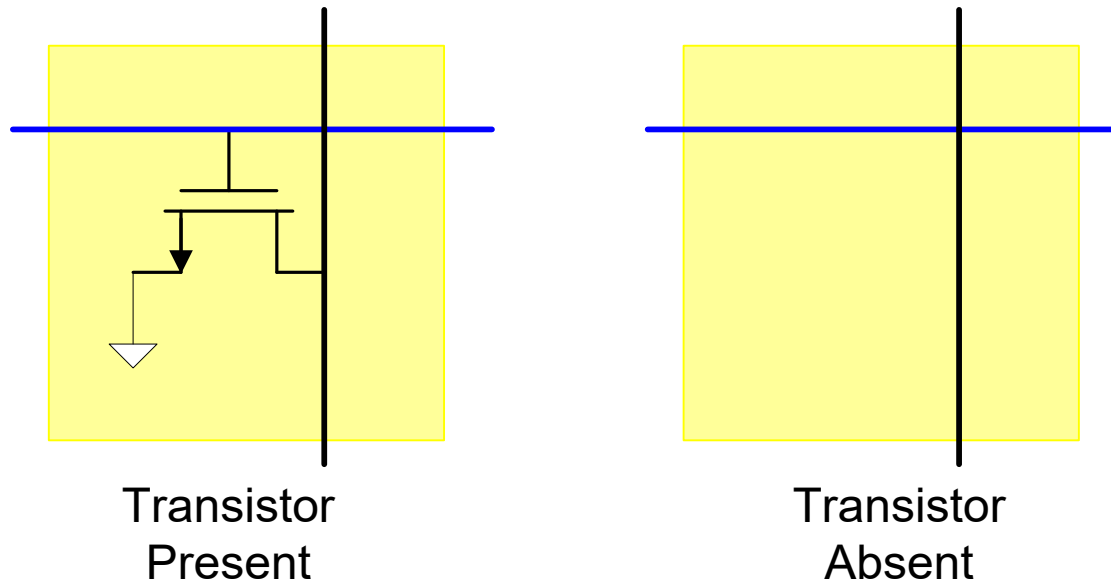
Mem Cells



Static RAM (SRAM)

- **Uses PTL and cross-coupled inverters**
- **Sizing of “switches” must be strong enough to write to cell**
- **No static power dissipation in this PTL implementation**

Mem Cells

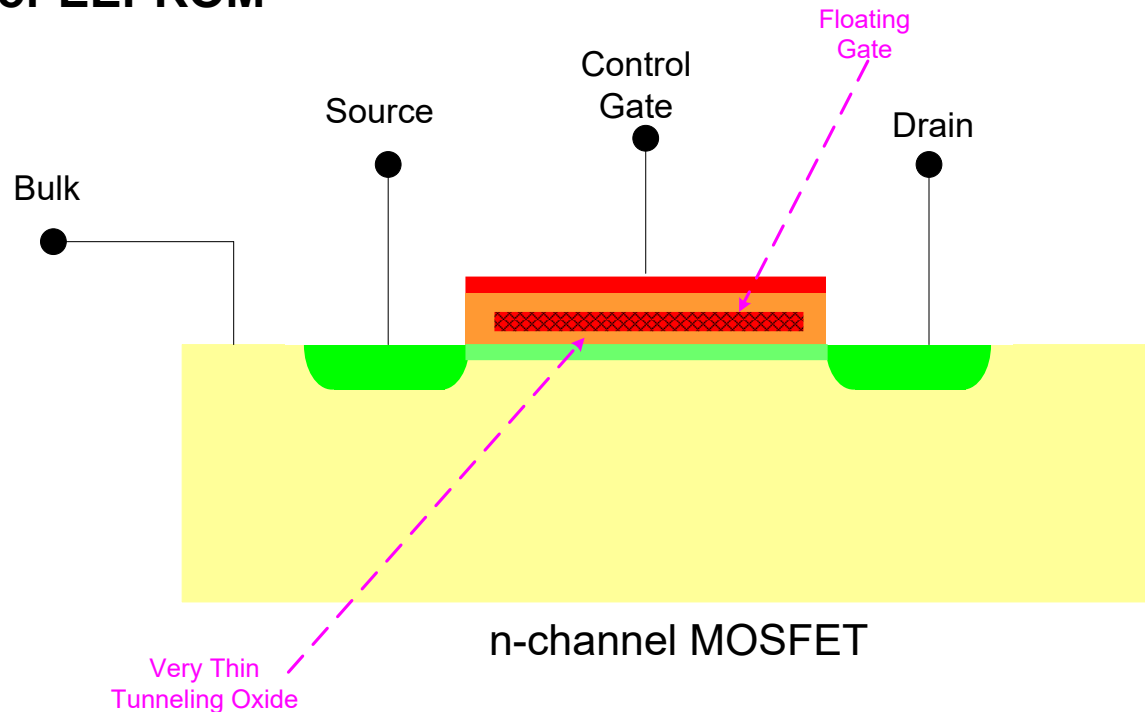


Static ROM (Mask programmable ROM)

- Site reserved for possible transistor
- Actually programmed with contact to gate and diffusion
- Can personalize with one or two masks
- Single transistor per bit
- Uses only one column line

Mem Cells

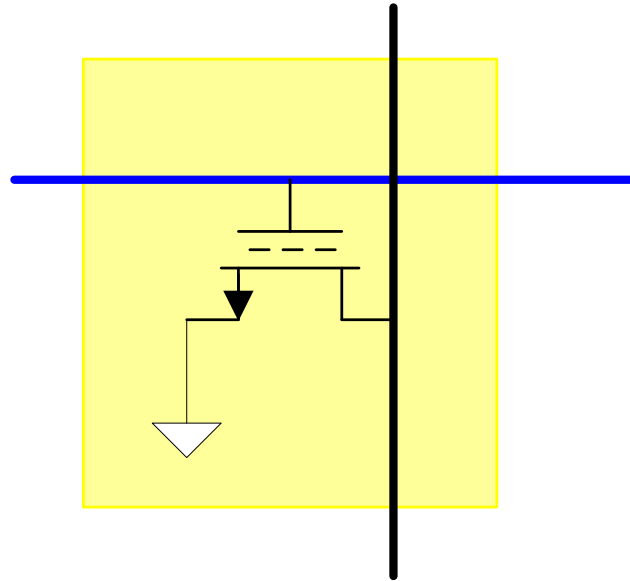
EPROM or EEPROM



Floating Gate Transistor

- Very thin floating gate
- Charge tunnels onto gate during programming to change V_T a lot
- Conceptual diagram only
- Somewhat specialized processing for reliable floating gate devices

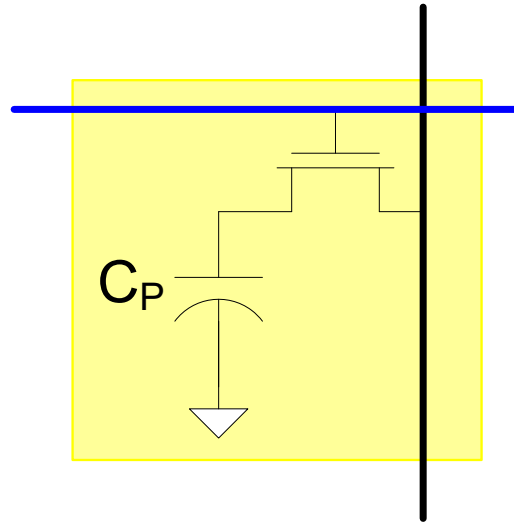
Mem Cells



EPROM or EEPROM

- **Floating Gate Transistor**
- **Programmed by Changing the Threshold Voltage**
- **Nonvolatile Memory**
- **Can be electrically programmed with EEPROM**
- **Limited number of read/write cycles (but enough for most applications)**
- **Uses only one column line**

Mem Cells



DRAM

- **Charge stored in small parasitic capacitor**
- **Very small cells**
- **Volatile and dynamic**
- **Special processes to make C_p large in very small area**
- **C_p is actually a part of the transistor**
- **Somewhat tedious architecture (details not shown) needed to sense very small charge**



Stay Safe and Stay Healthy !

End of Lecture 44